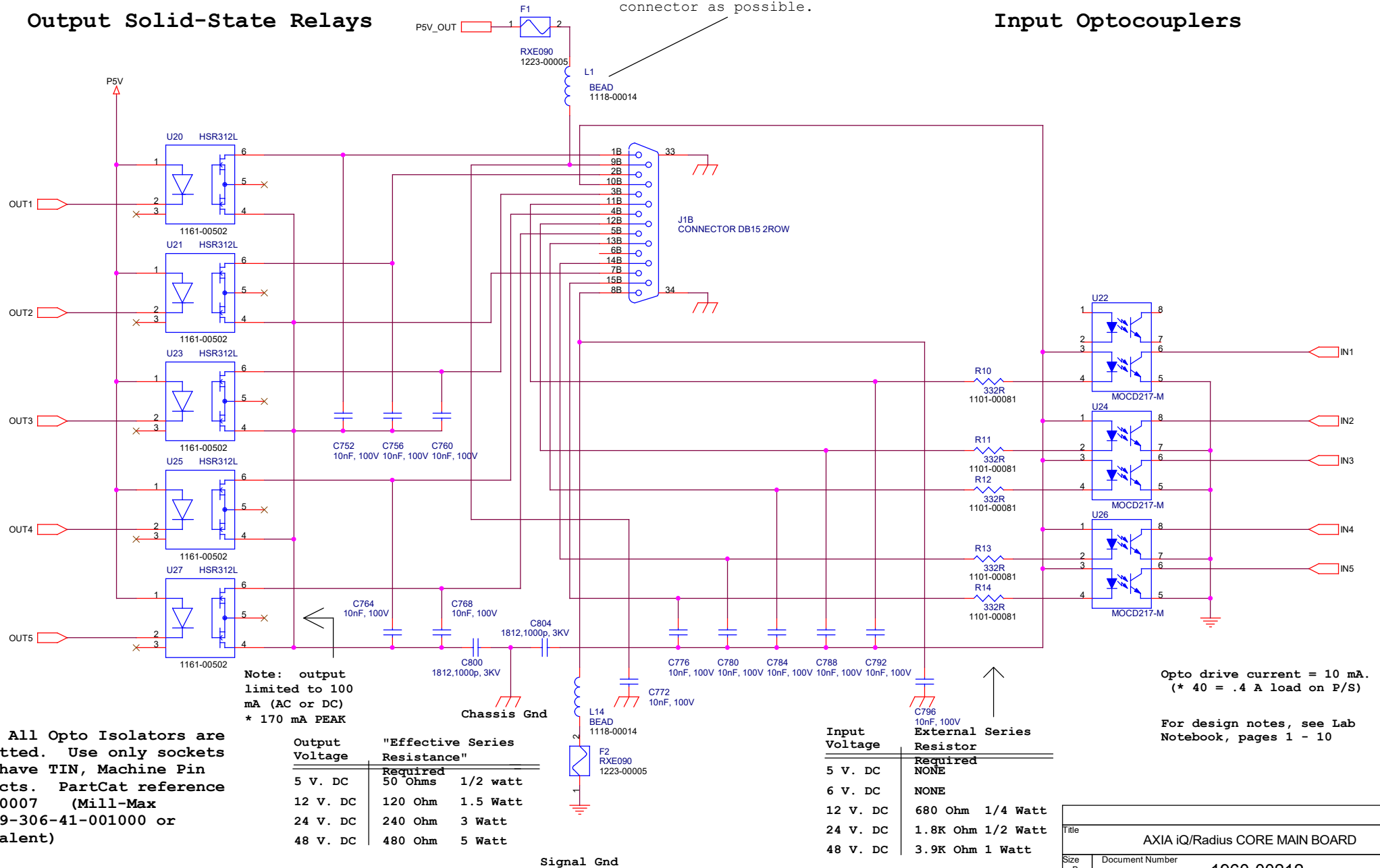


Output Solid-State Relays

NOTE: All EMI filters are to be located as close to the 15-pin D connector as possible.

Input Optocouplers

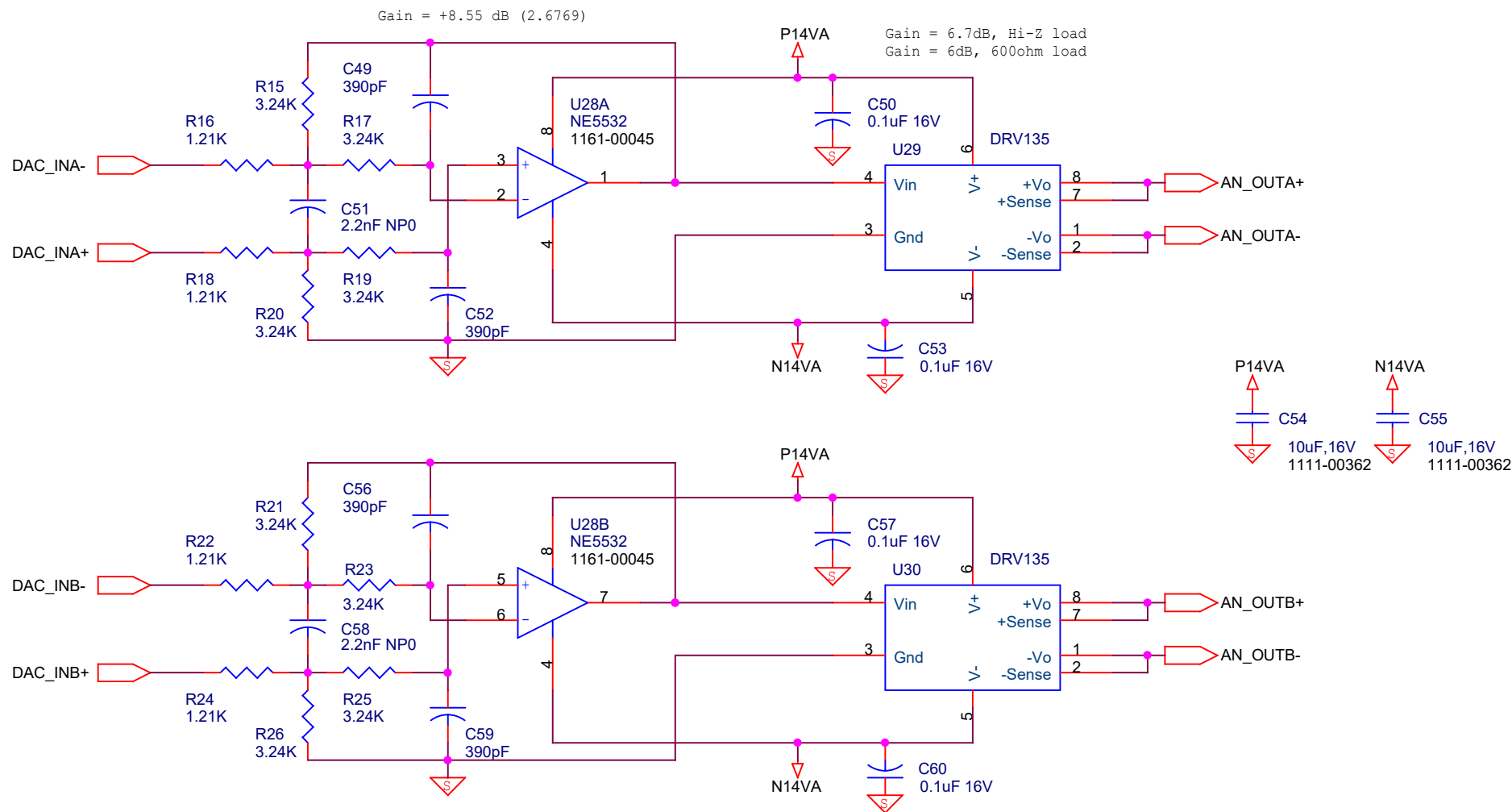


Title			AXIA iQ/Radius CORE MAIN BOARD		
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0 dBFS = 6.5 VPP = 2.3 VRMS

0 dBFS = 17.40 VPP = 6.15 VRMS

0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

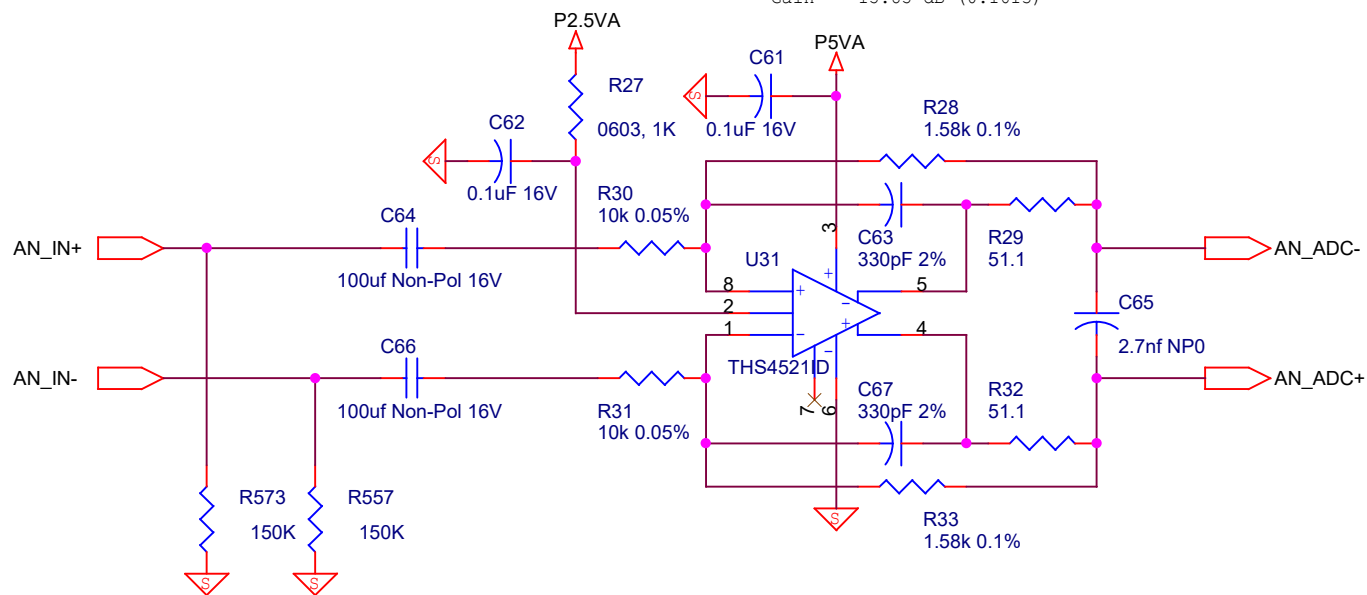


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

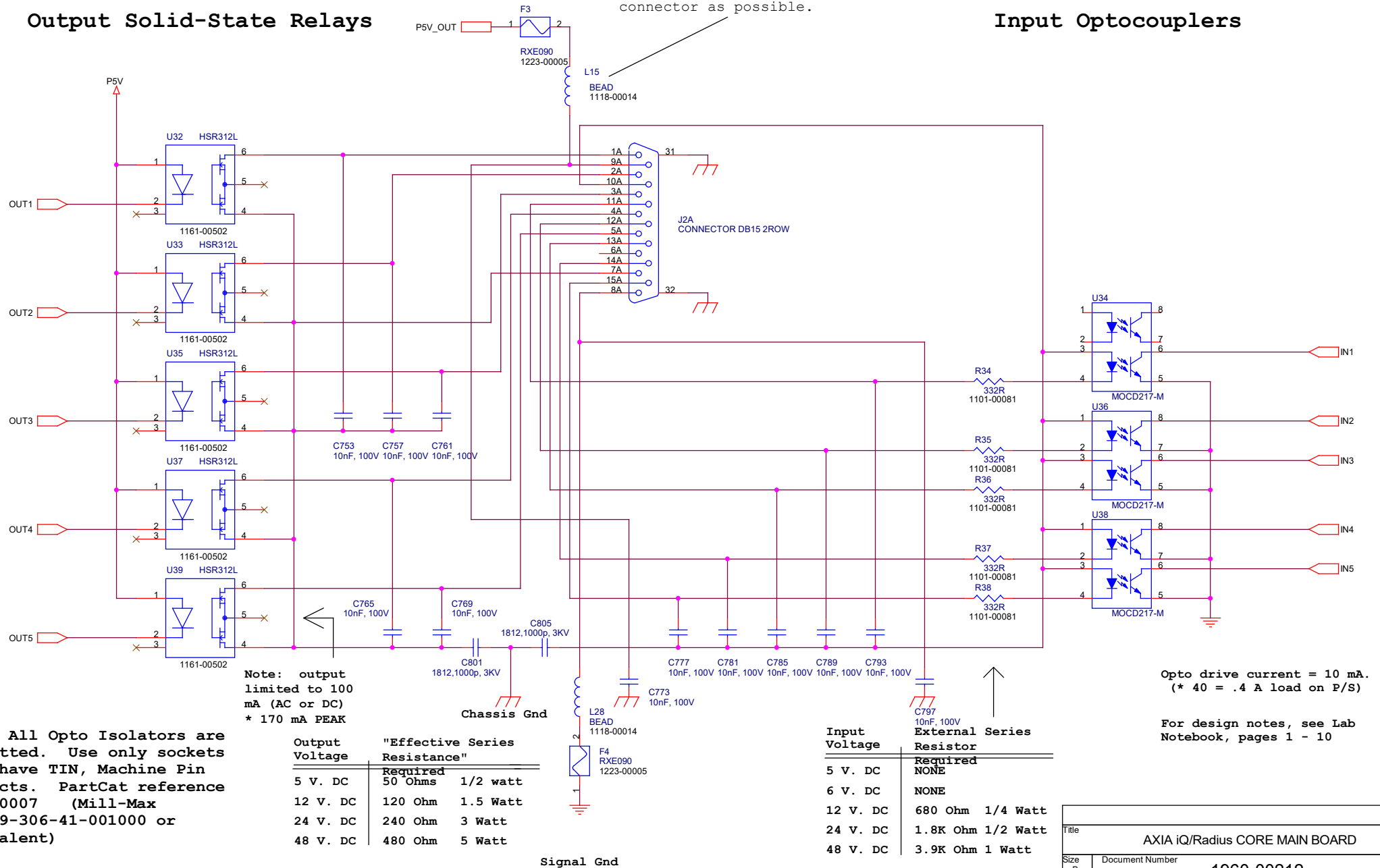


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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Output Solid-State Relays

NOTE: All EMI filters are to be located as close to the 15-pin D connector as possible.

Input Optocouplers

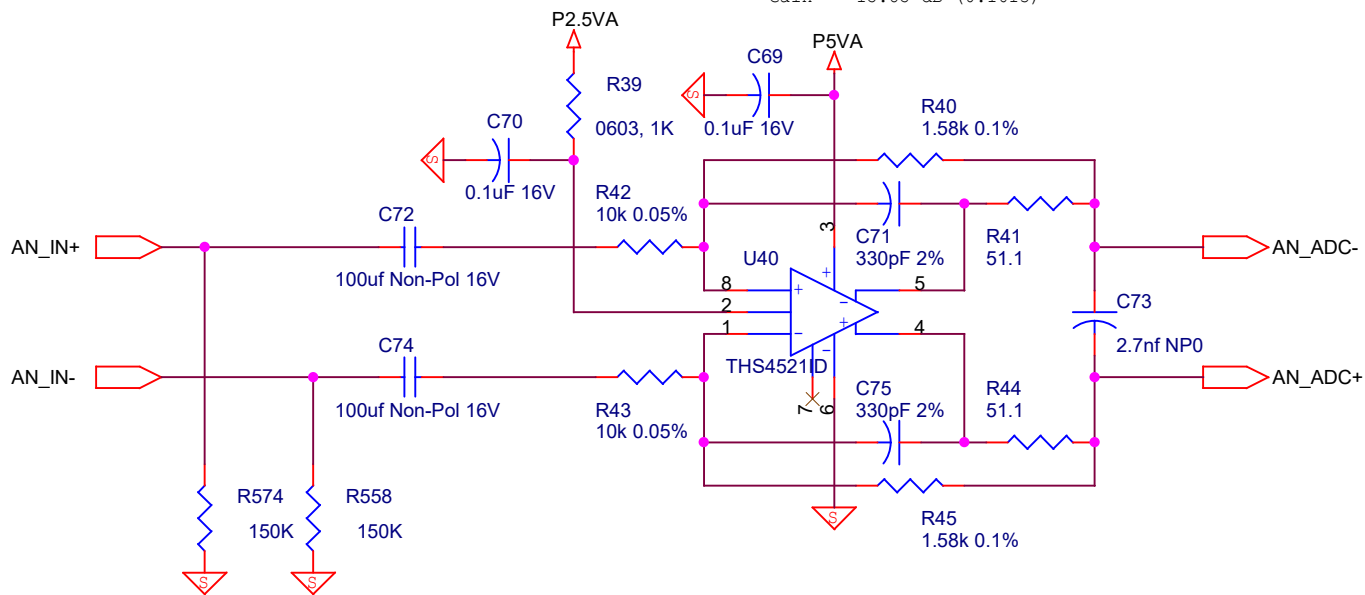


Title			AXIA iQ/Radius CORE MAIN BOARD	
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

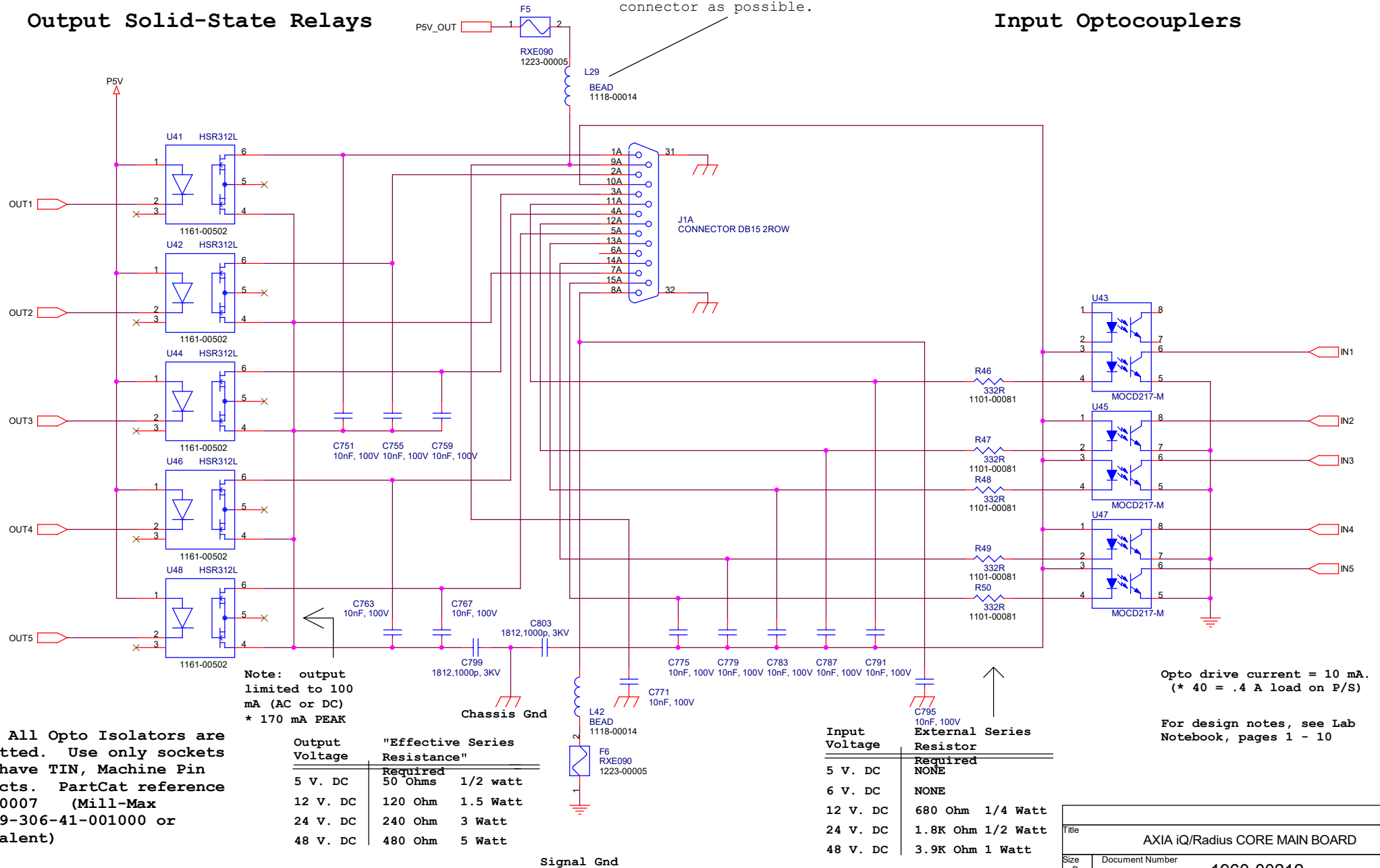


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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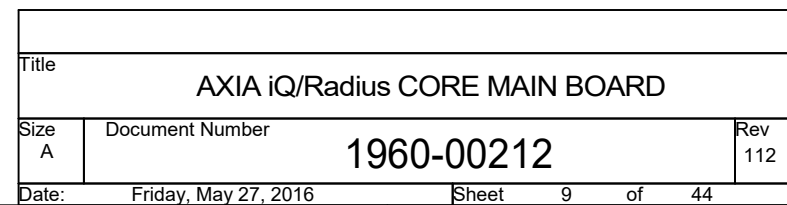
Output Solid-State Relays

NOTE: All EMI filters are to be located as close to the 15-pin D connector as possible.

Input Optocouplers



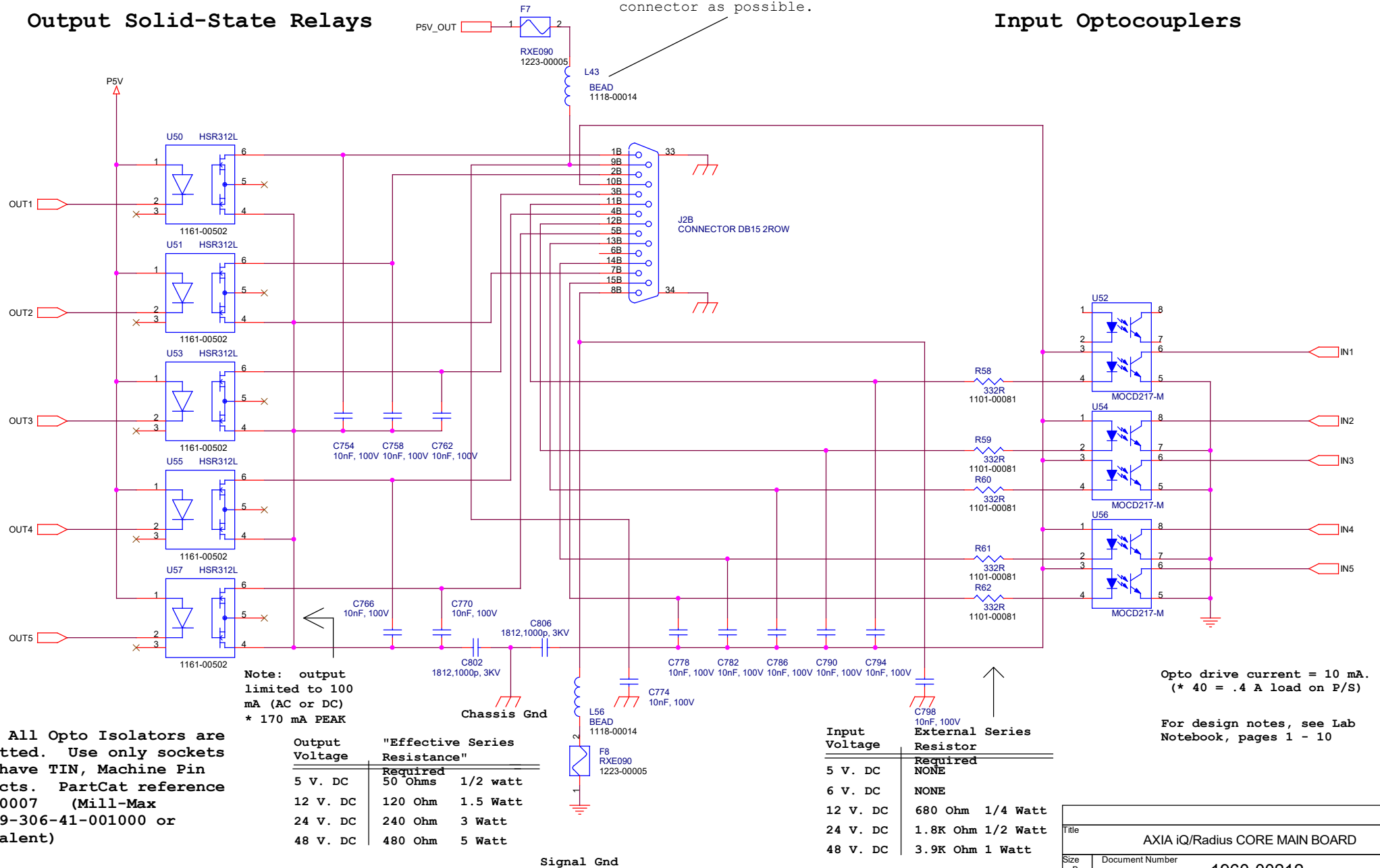
Title			AXIA iQ/Radius CORE MAIN BOARD
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$$0 \text{ dBFS} = 5.6 \text{ VPP} = 1.98 \text{ VRMS}$$


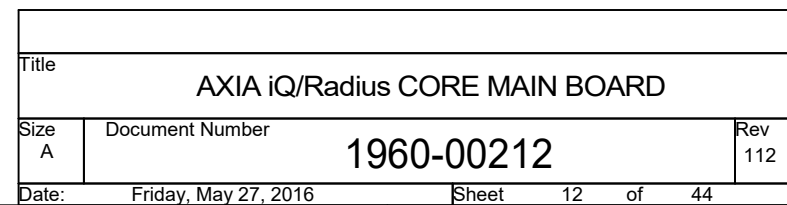
Output Solid-State Relays

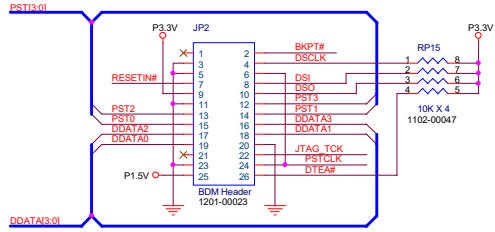
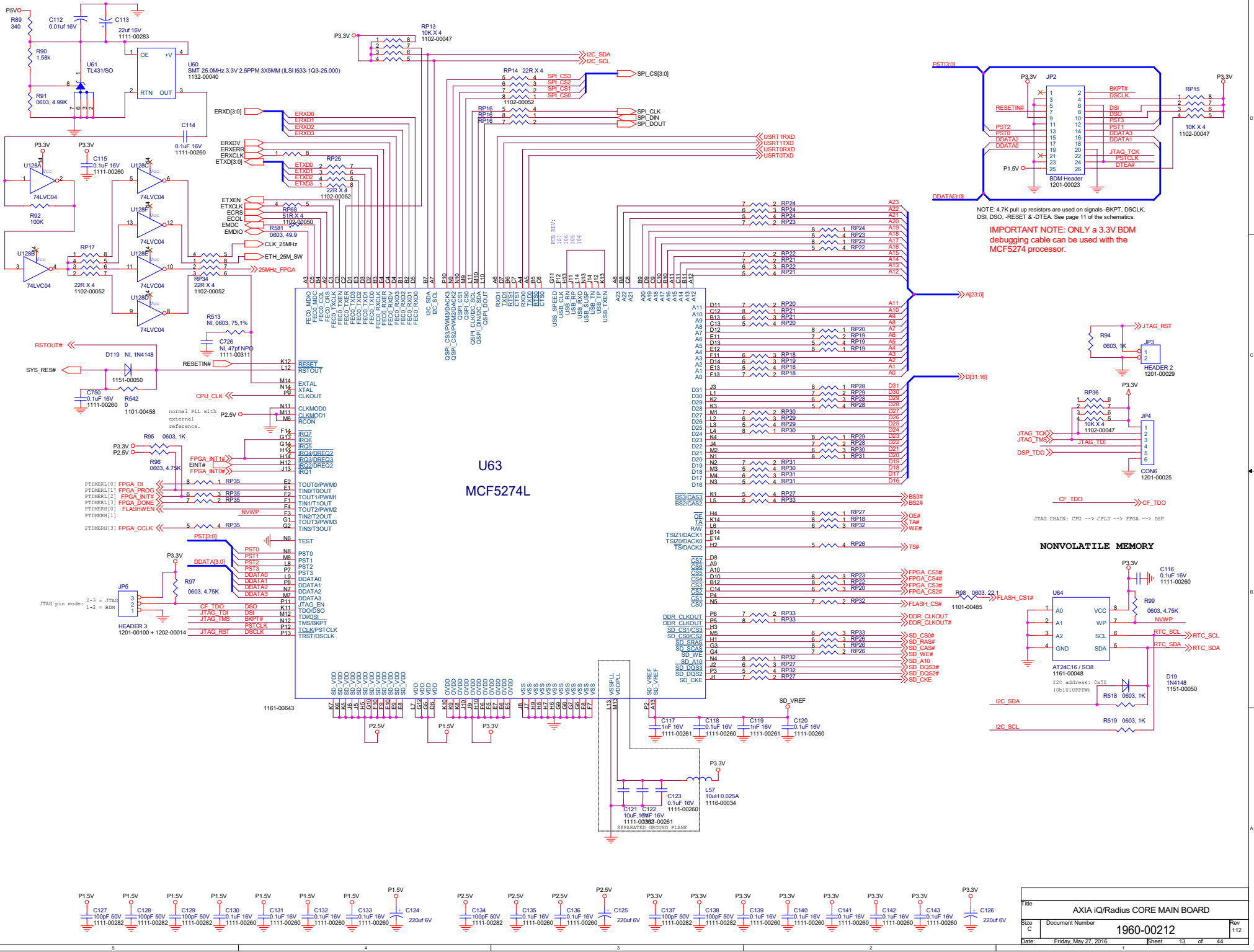
NOTE: All EMI filters are to be located as close to the 15-pin D connector as possible.

Input Optocouplers



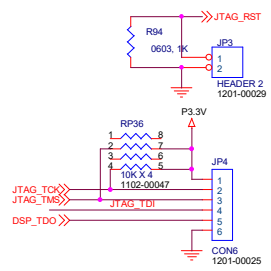
Title			AXIA iQ/Radius CORE MAIN BOARD
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$$0 \text{ dBFS} = 5.6 \text{ VPP} = 1.98 \text{ VRMS}$$


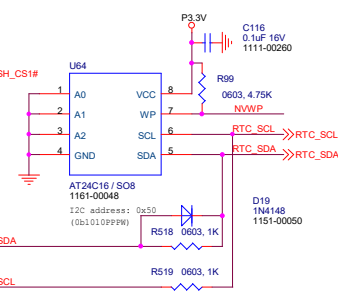


NOTE: 4.7K pull up resistors are used on signals -BKPT#, DSCLK, DSI, DSO, -RESET# & -DTEA. See page 11 of the schematics.

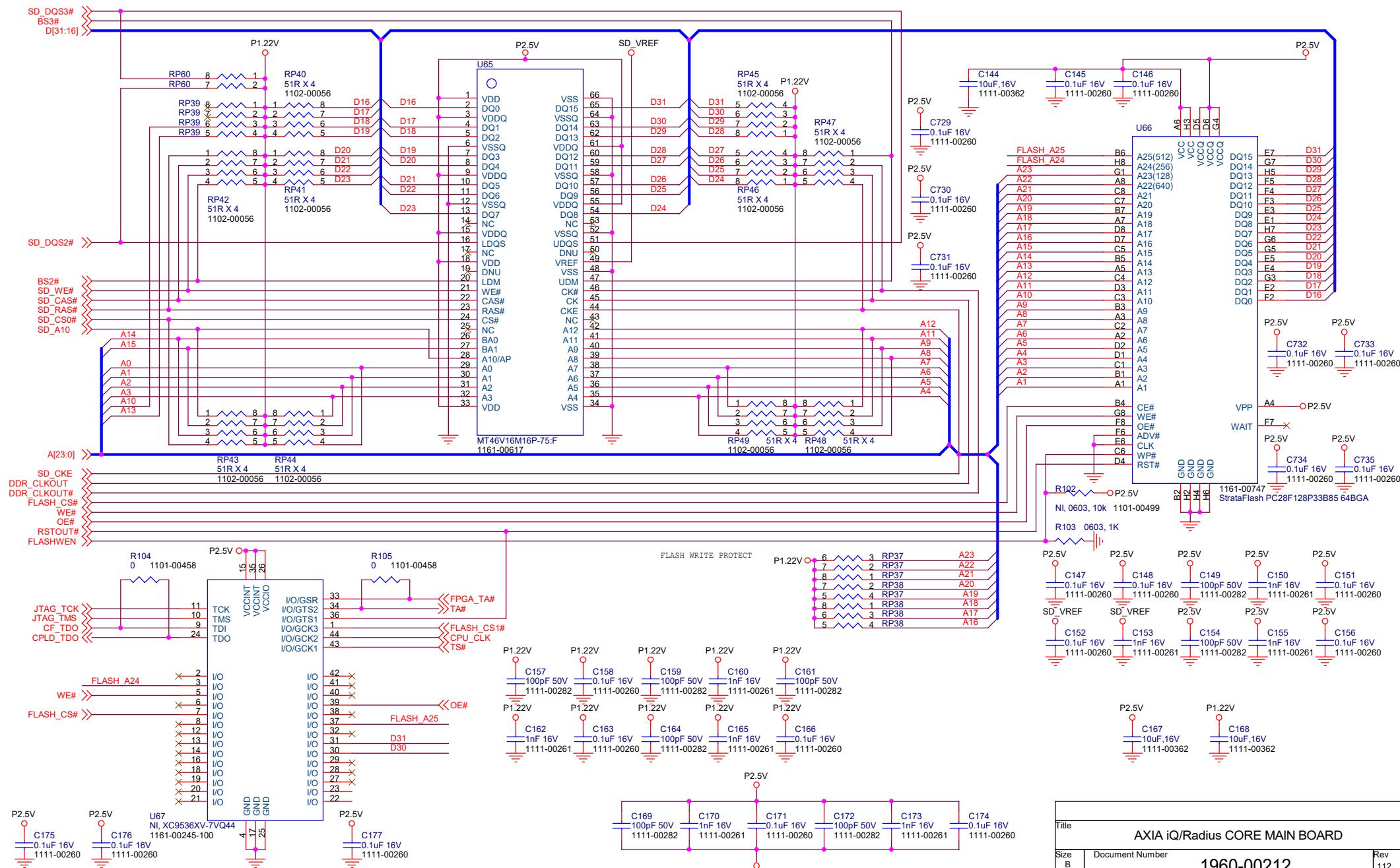
IMPORTANT NOTE: ONLY a 3.3V BDM debugging cable can be used with the MCF5274 processor.



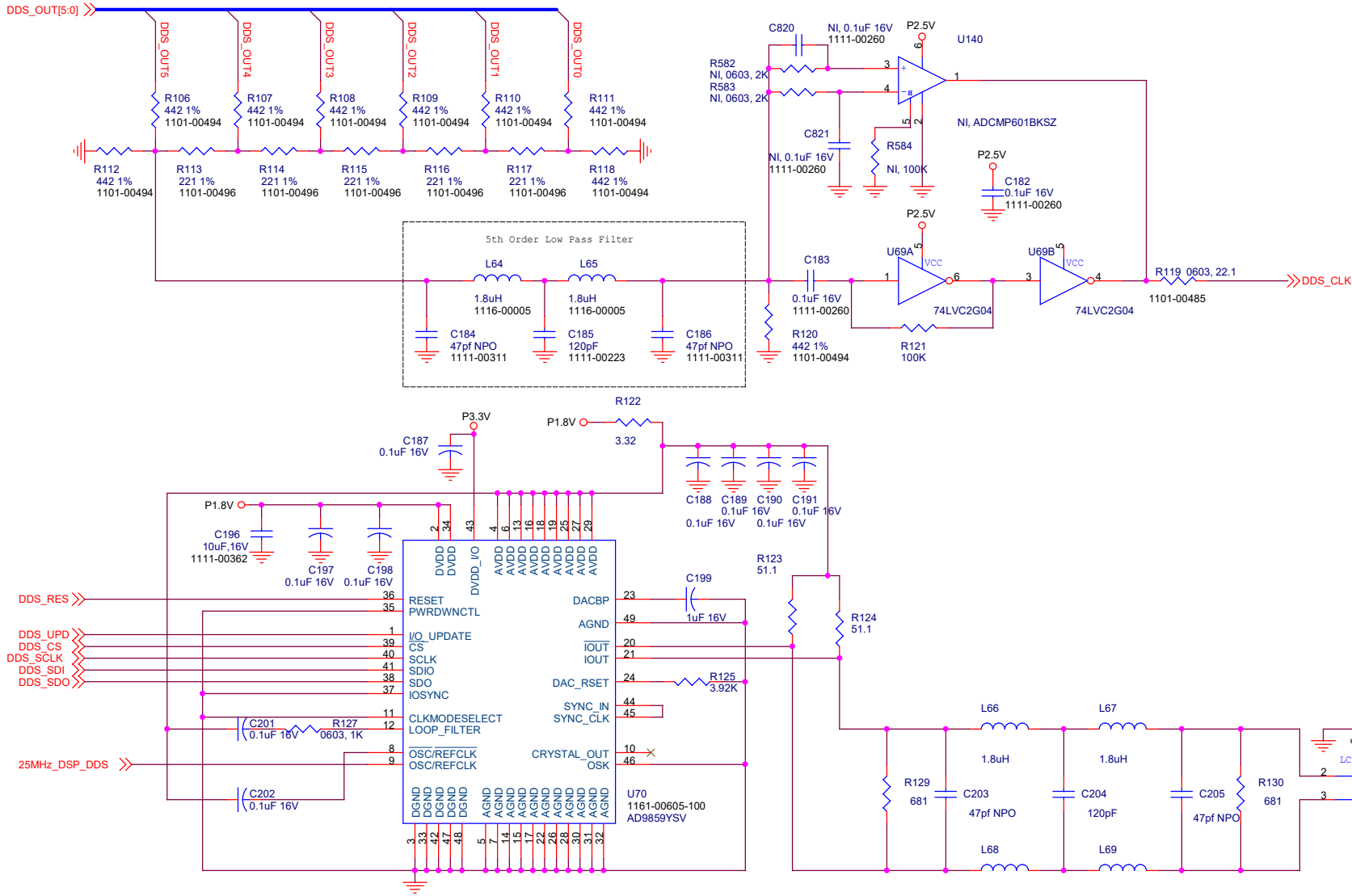
NONVOLATILE MEMORY



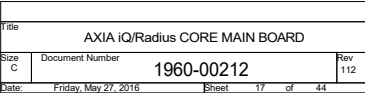
AXIA iQ/Radius CORE MAIN BOARD			
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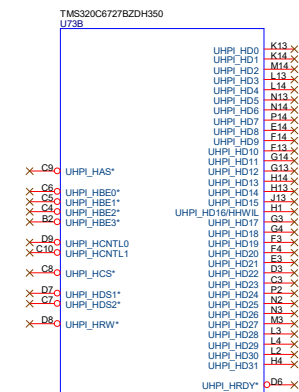
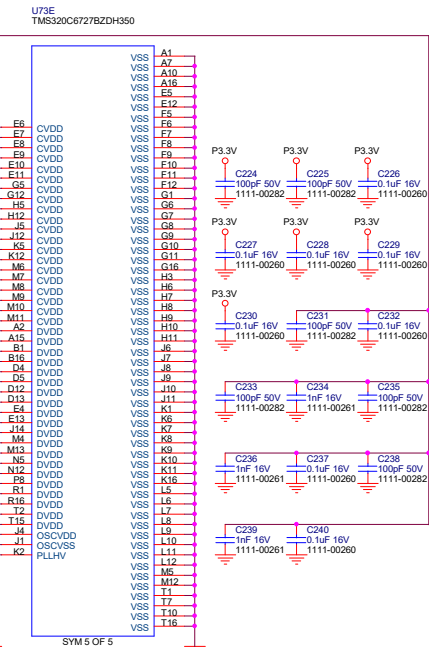
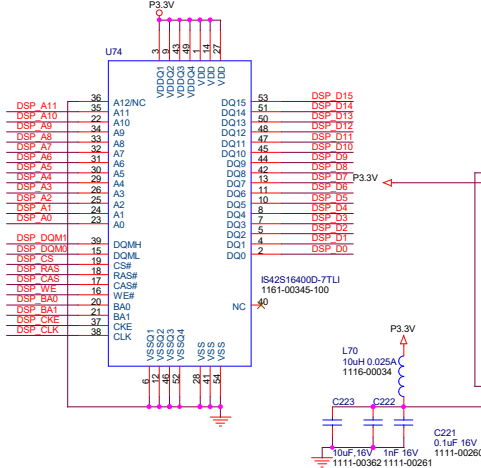
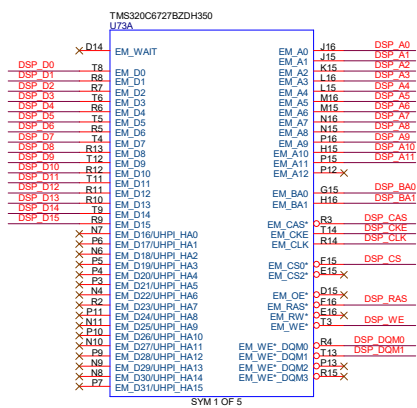
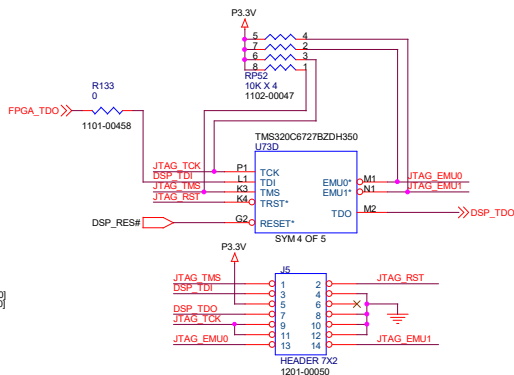
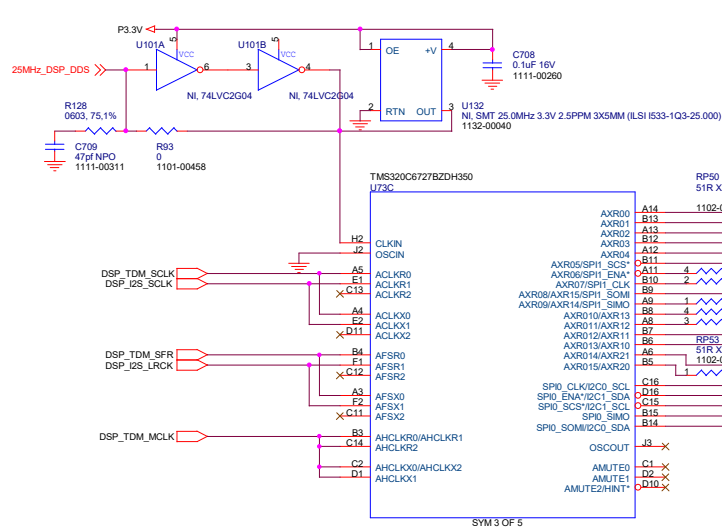


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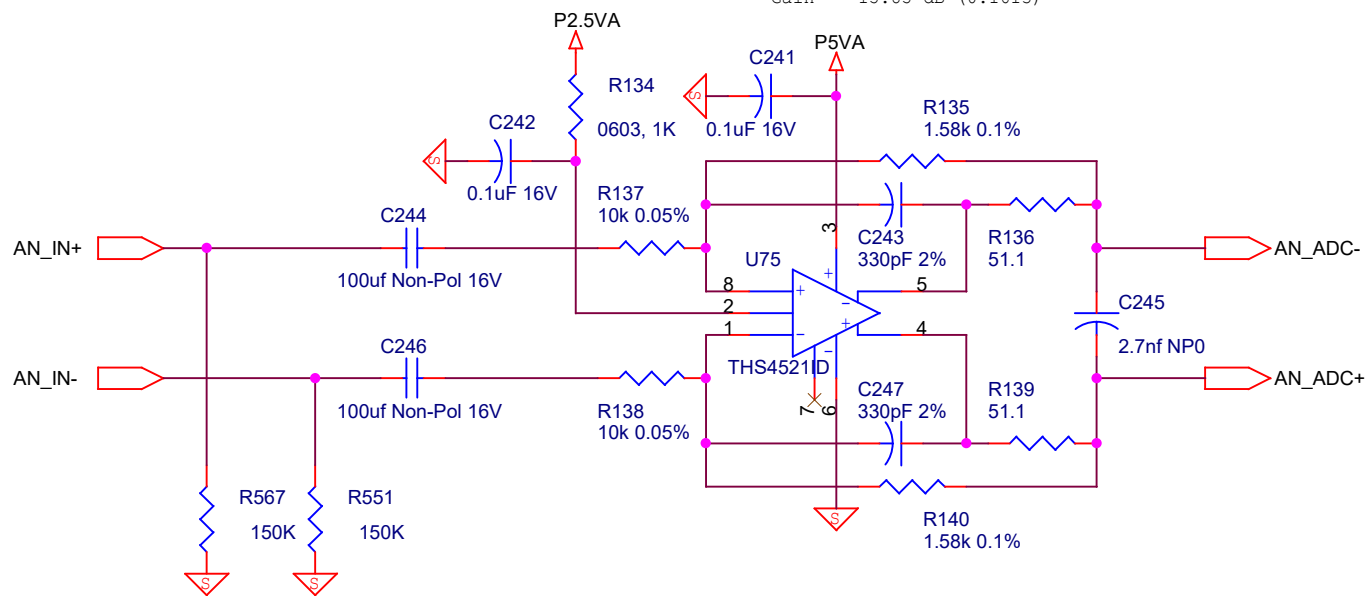




0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

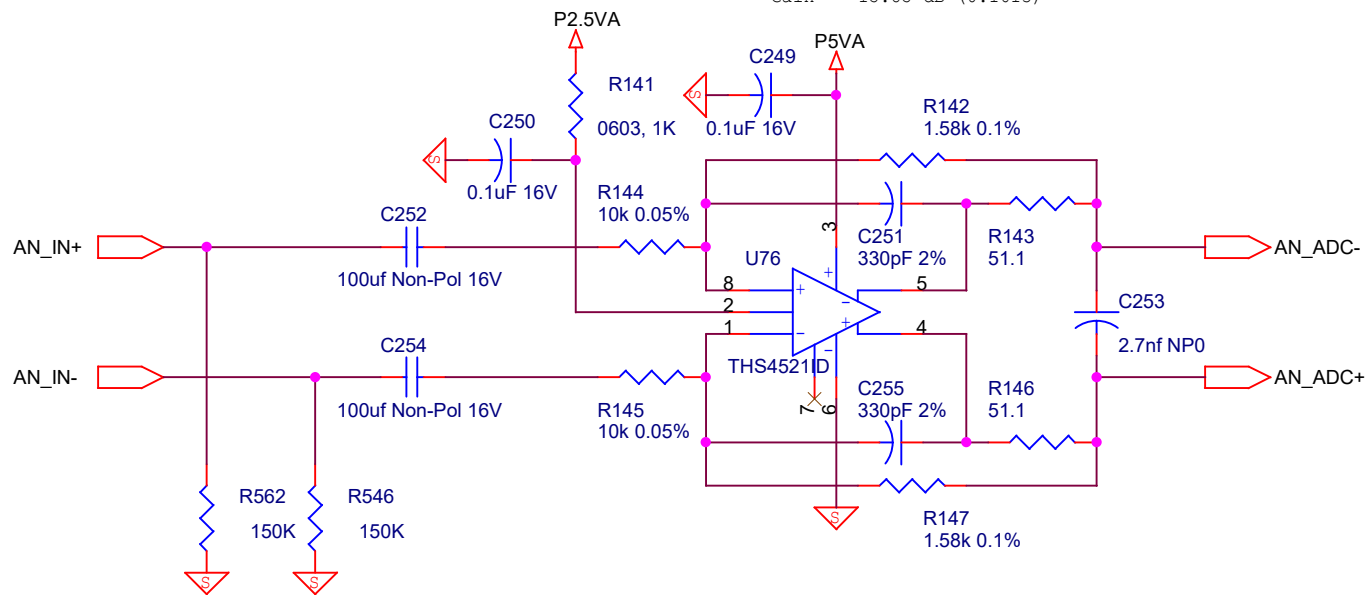


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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

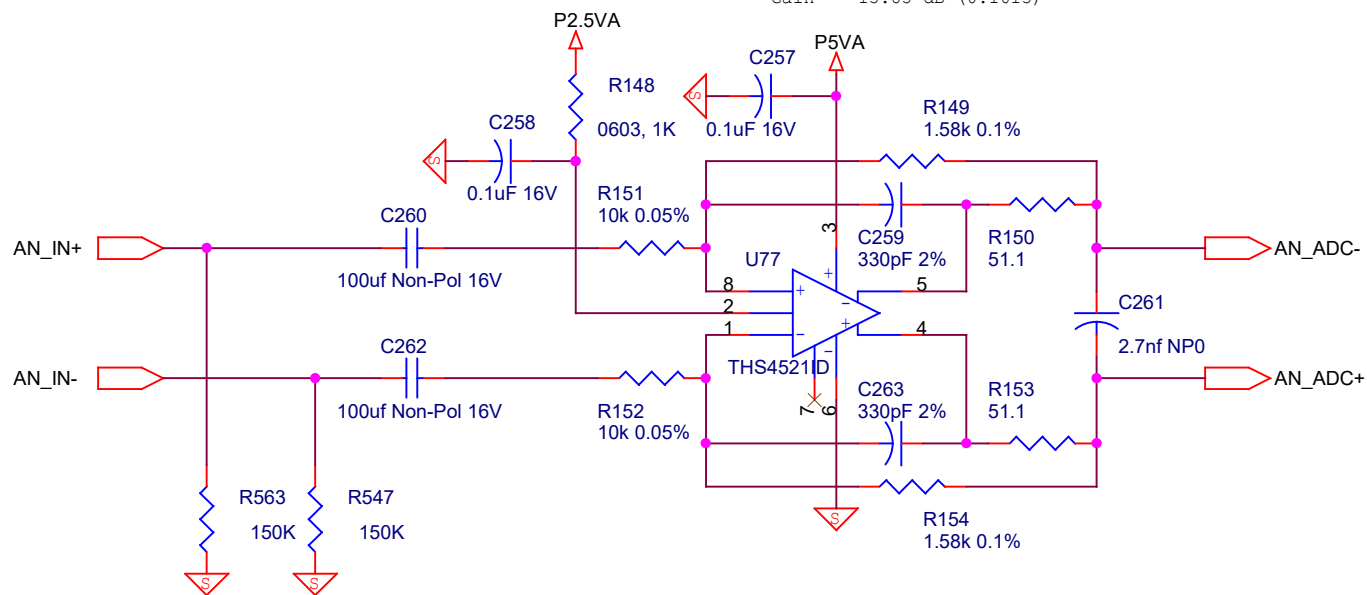


Title		
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

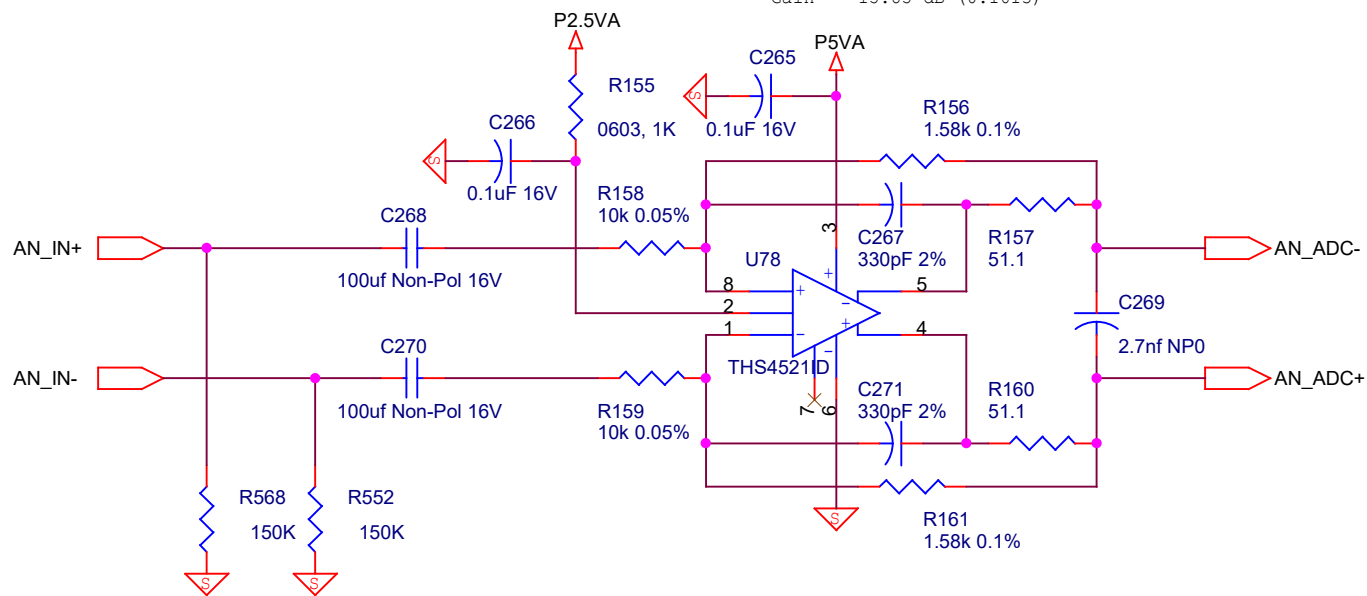


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

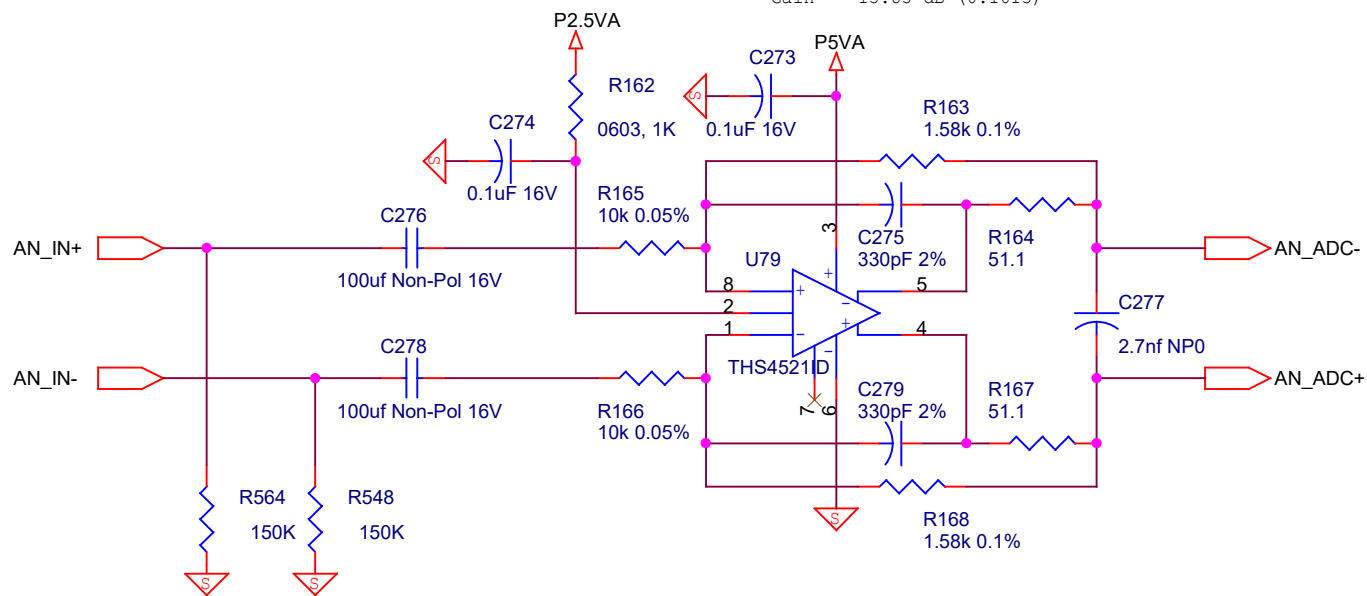


Title		
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

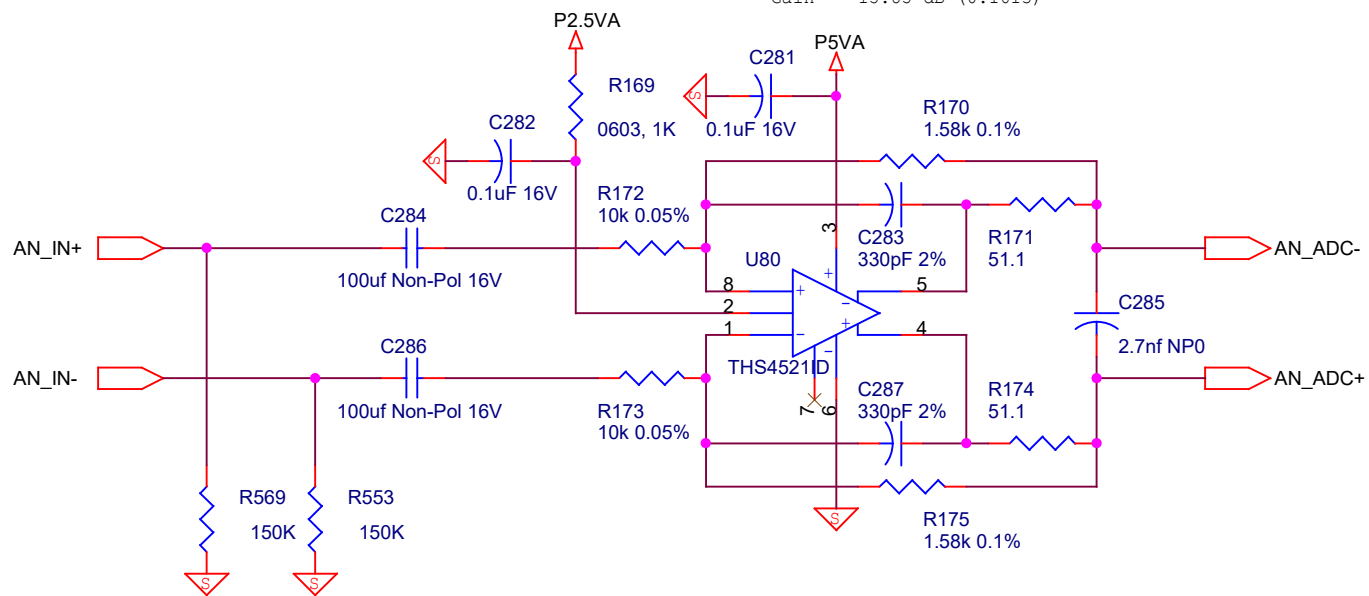


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

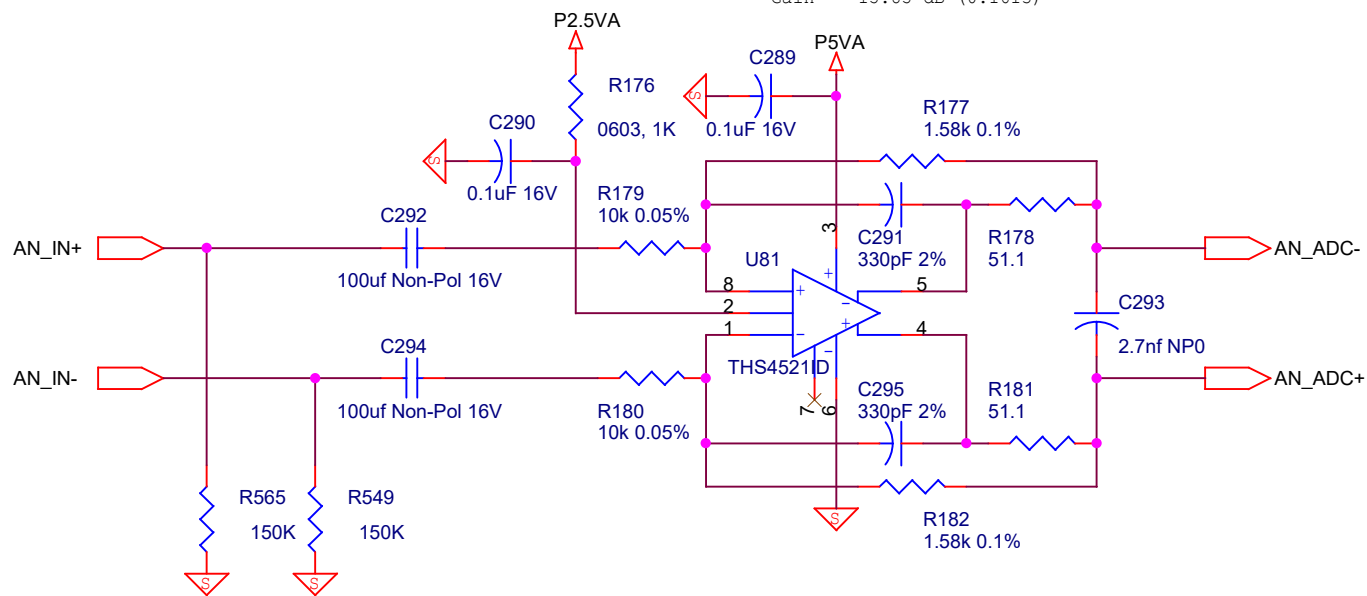


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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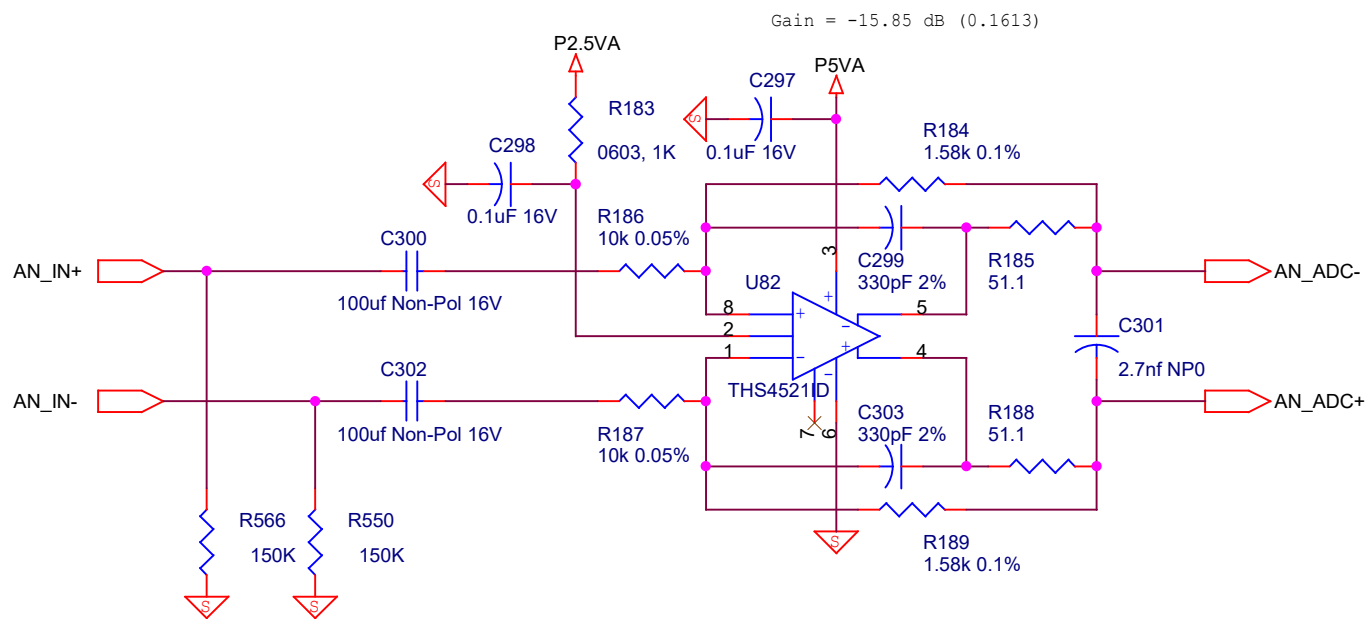
0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)



Title		
AXIA iQ/Radius CORE MAIN BOARD		
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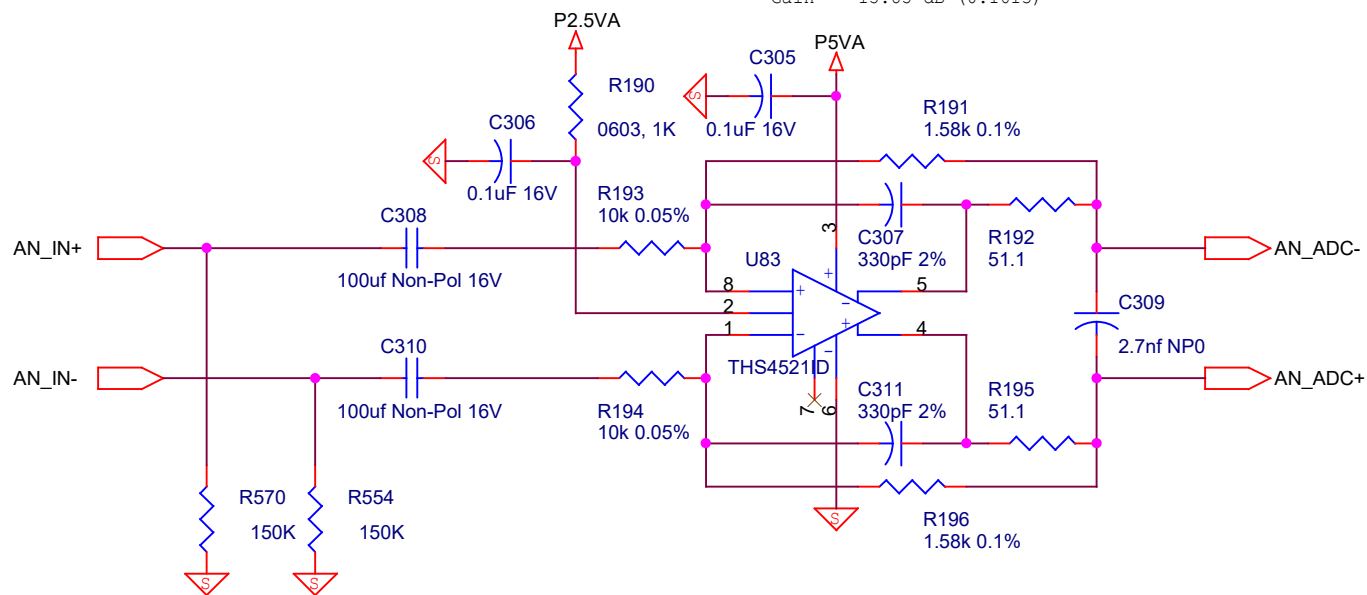
$$0 \text{ dBFS} = 5.6 \text{ VPP} = 1.98 \text{ VRMS}$$


Title AXIA iQ/Radius CORE MAIN BOARD			
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0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)

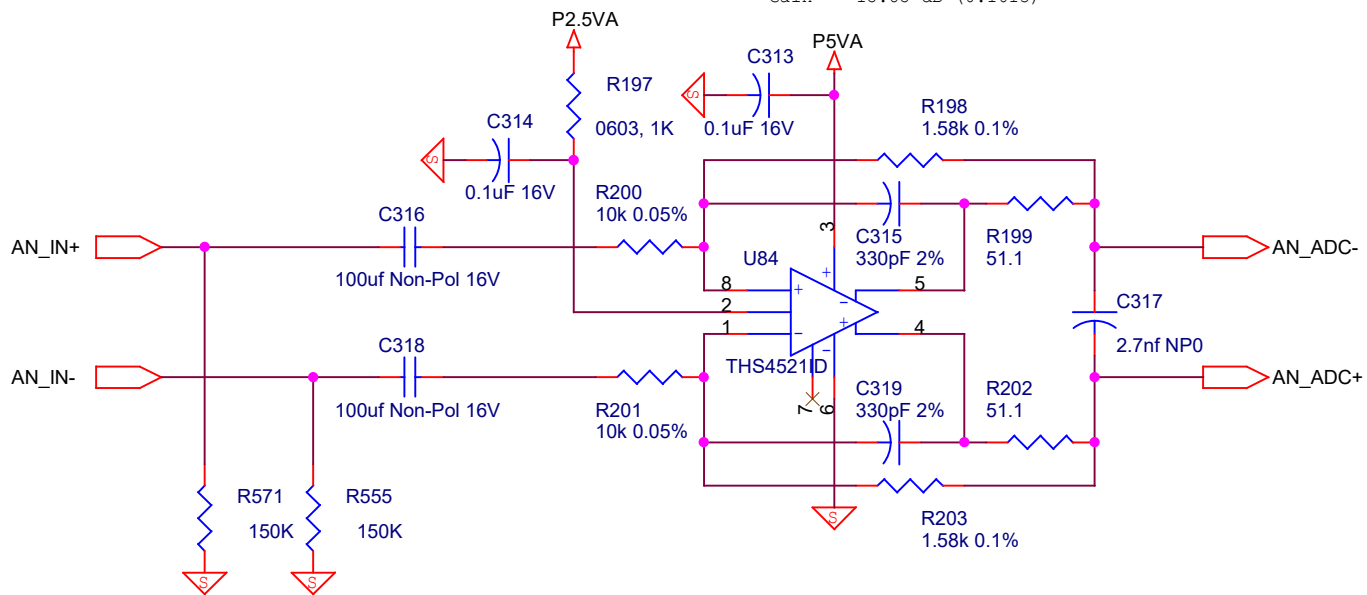


Title		
AXIA iQ/Radius CORE MAIN BOARD		
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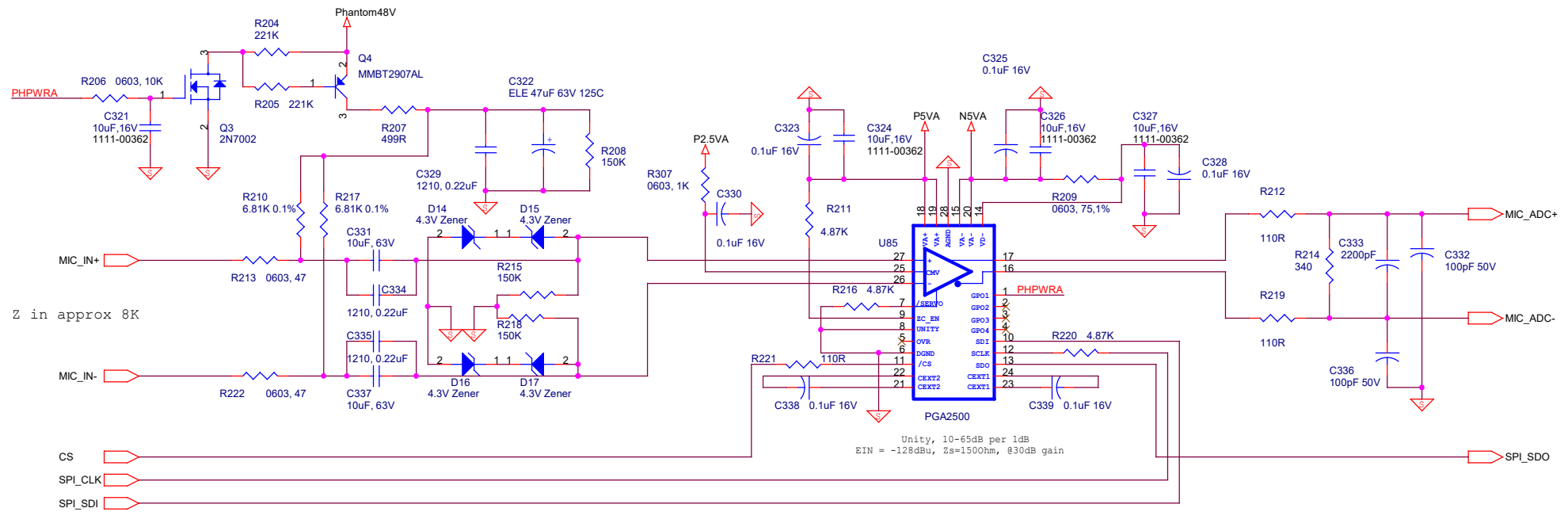
0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

Gain = -15.85 dB (0.1613)



Title		
AXIA iQ/Radius CORE MAIN BOARD		
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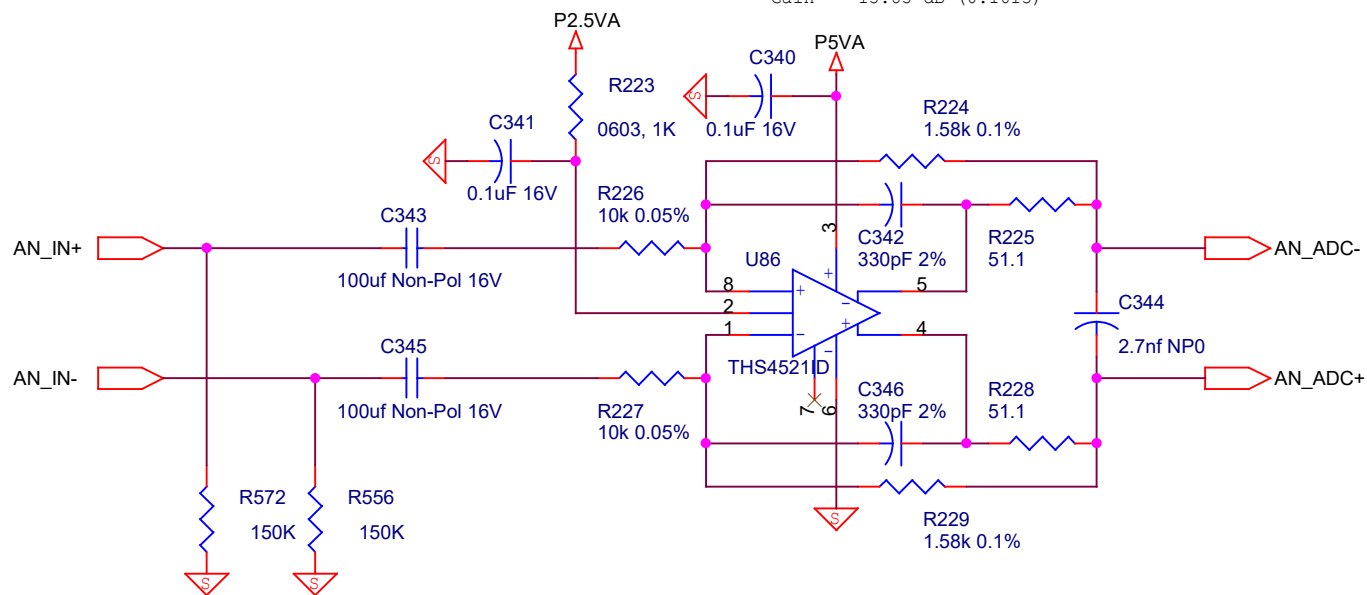


Title		
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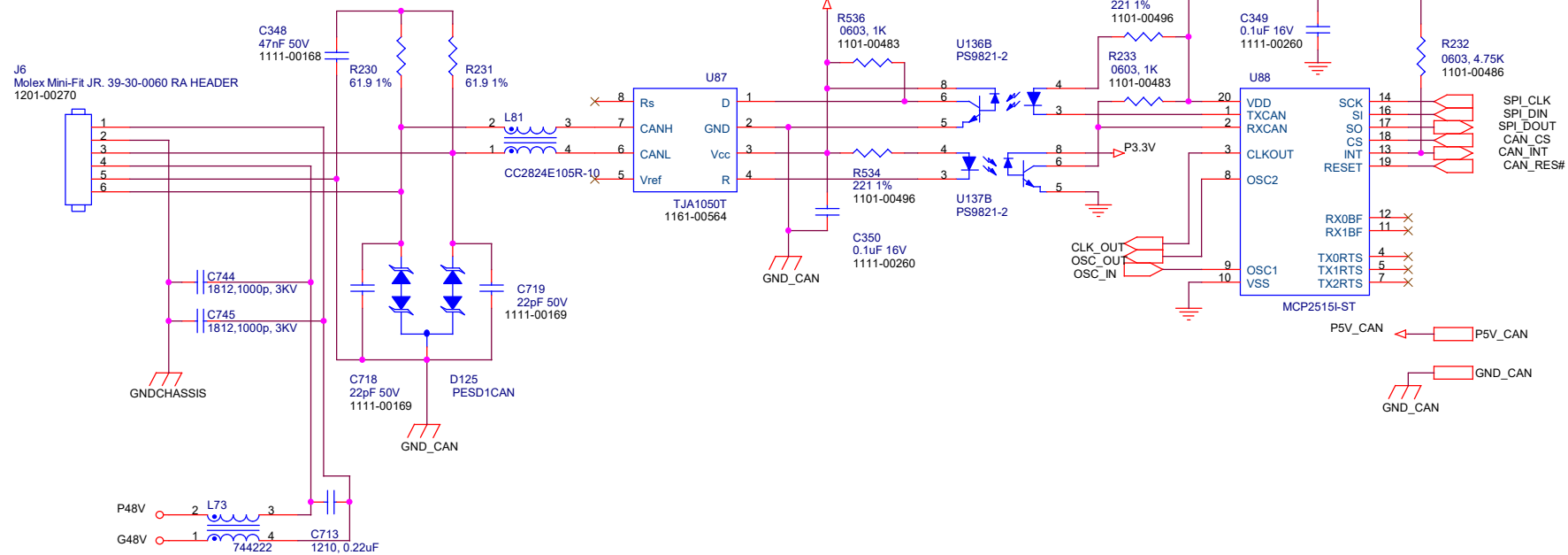
0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

0 dBFS = 5.6 VPP = 1.98 VRMS

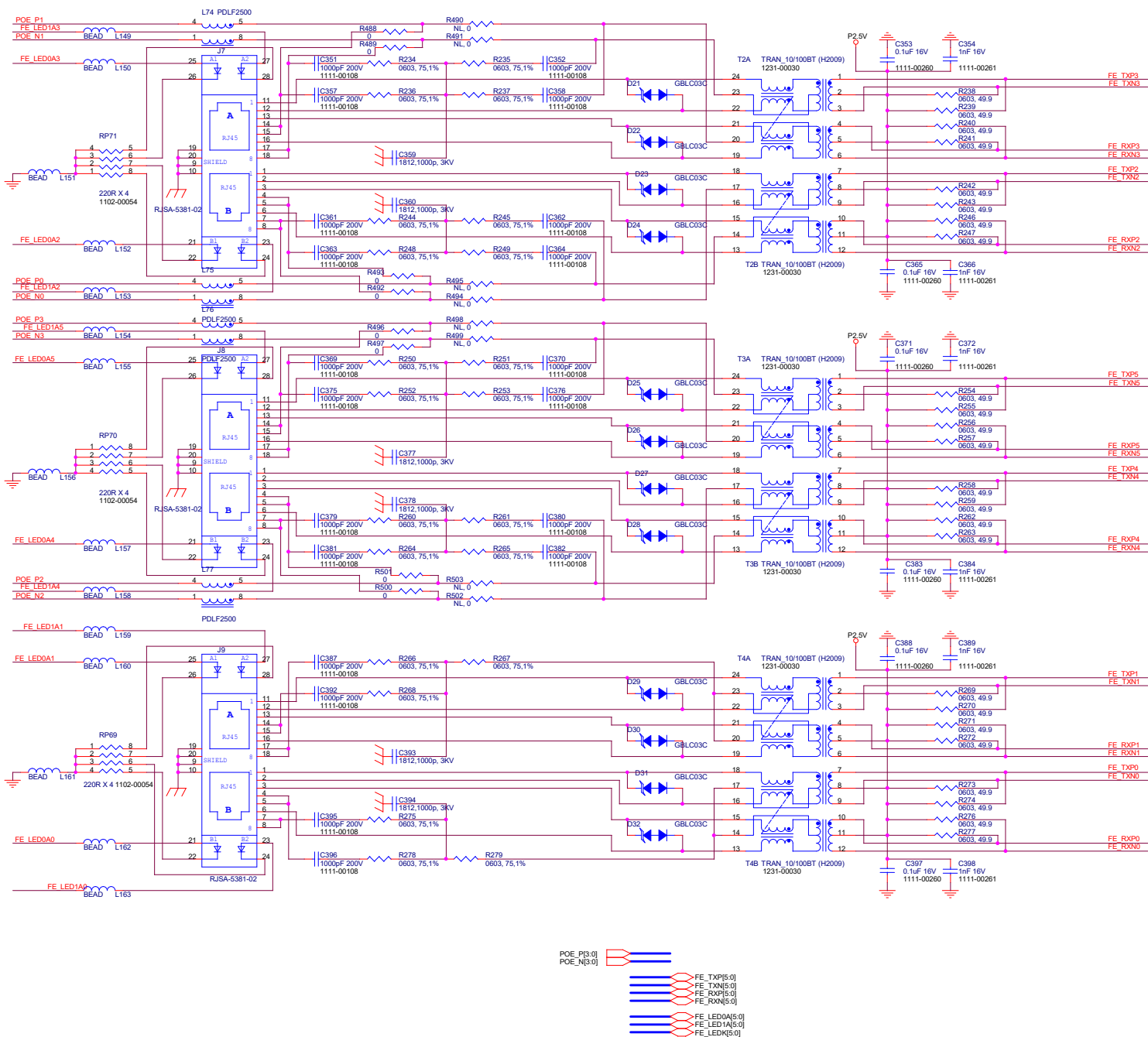
Gain = -15.85 dB (0.1613)



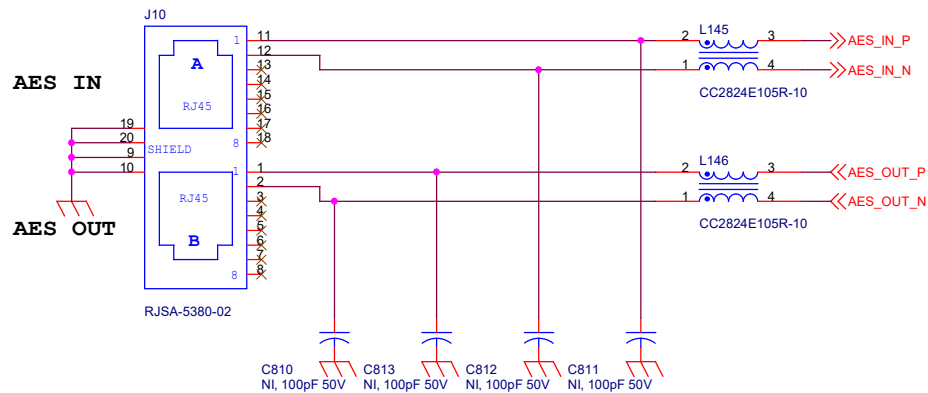
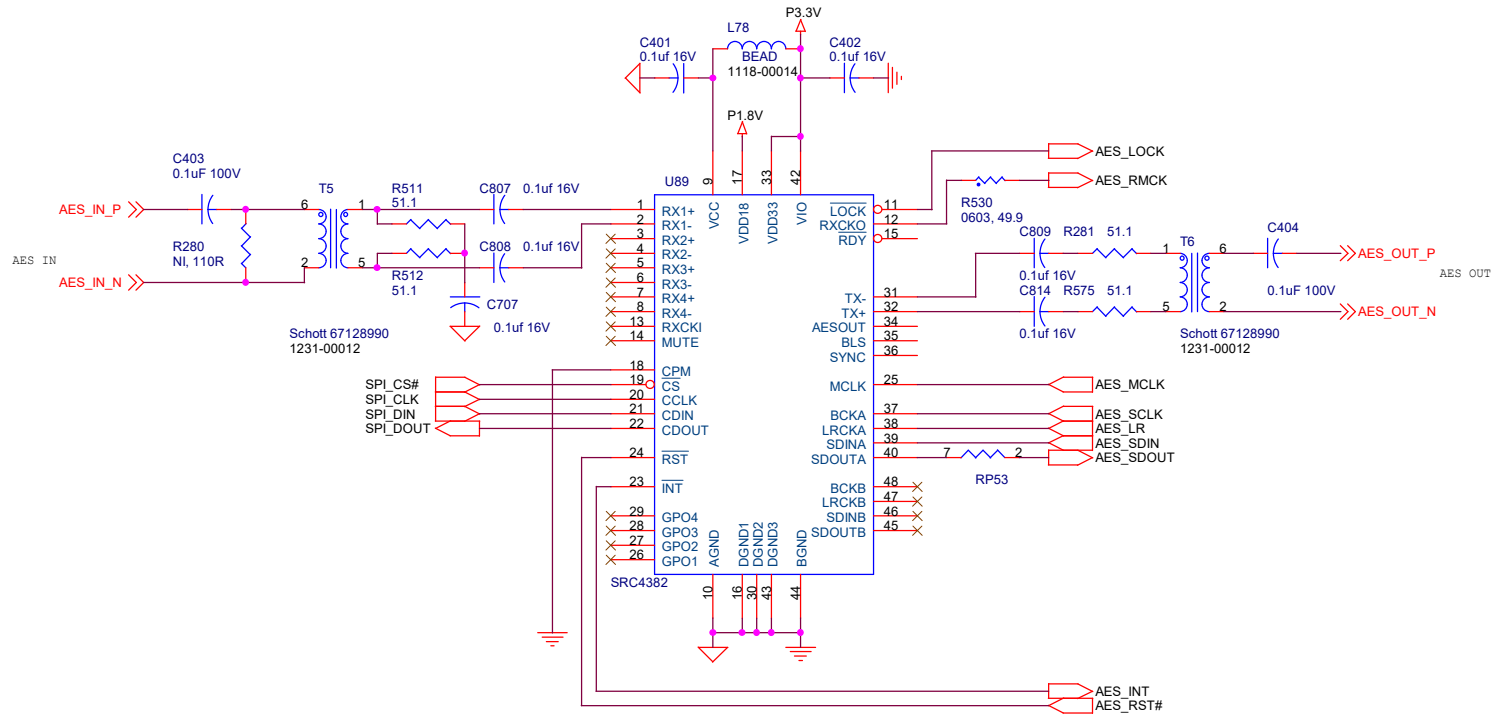
Title		
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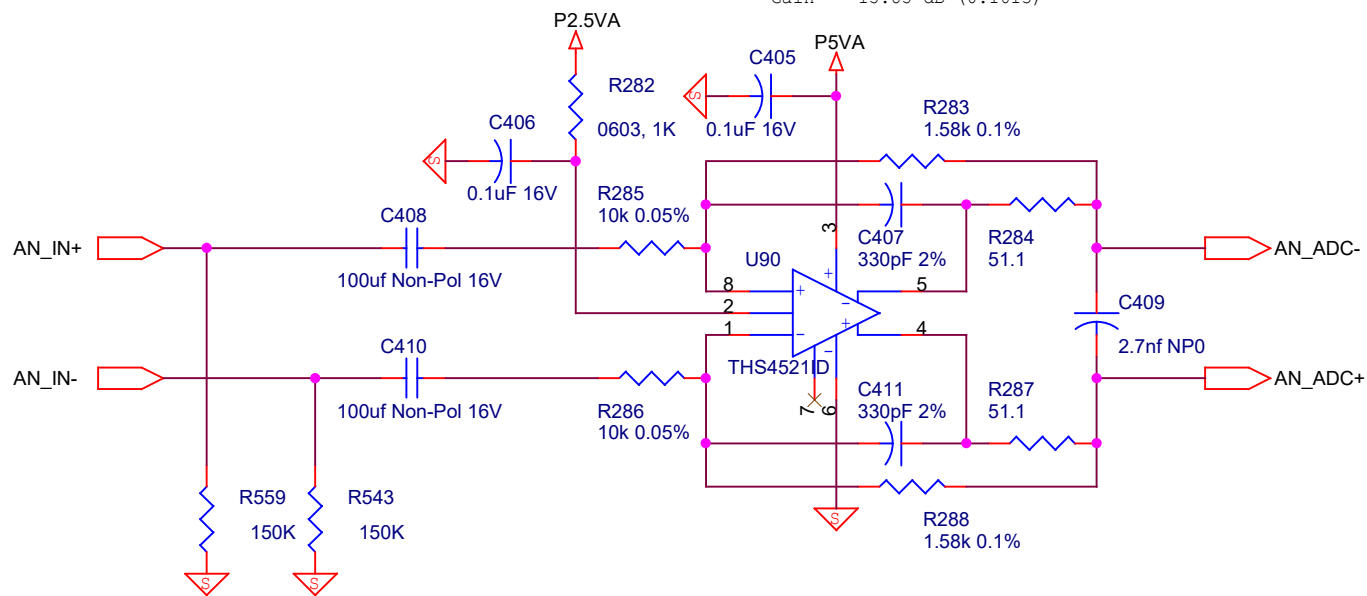


Title			
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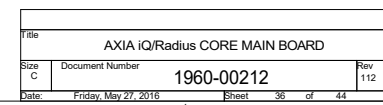
0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

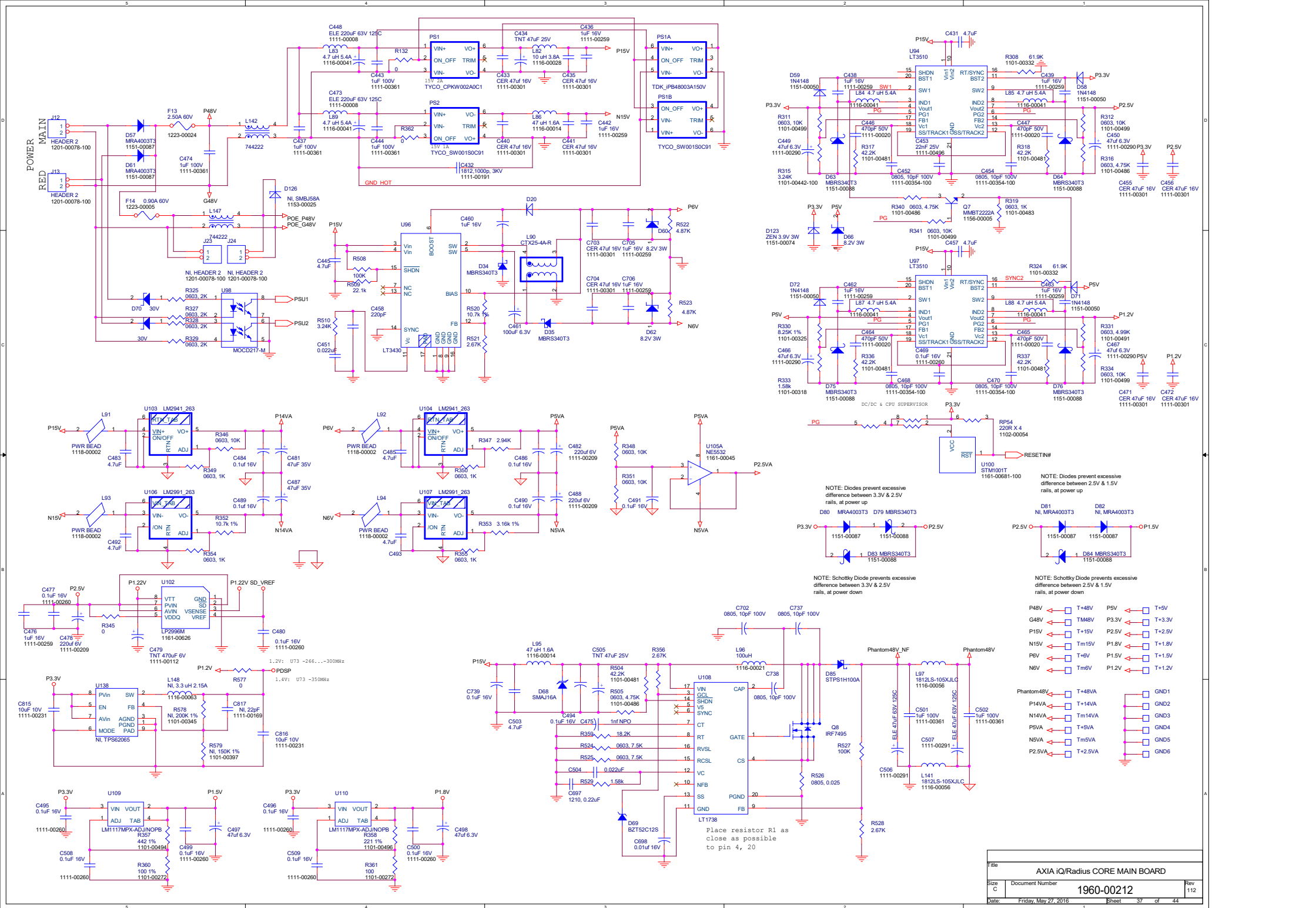
0 dBFS = 5.6 VPP = 1.98 VRMS

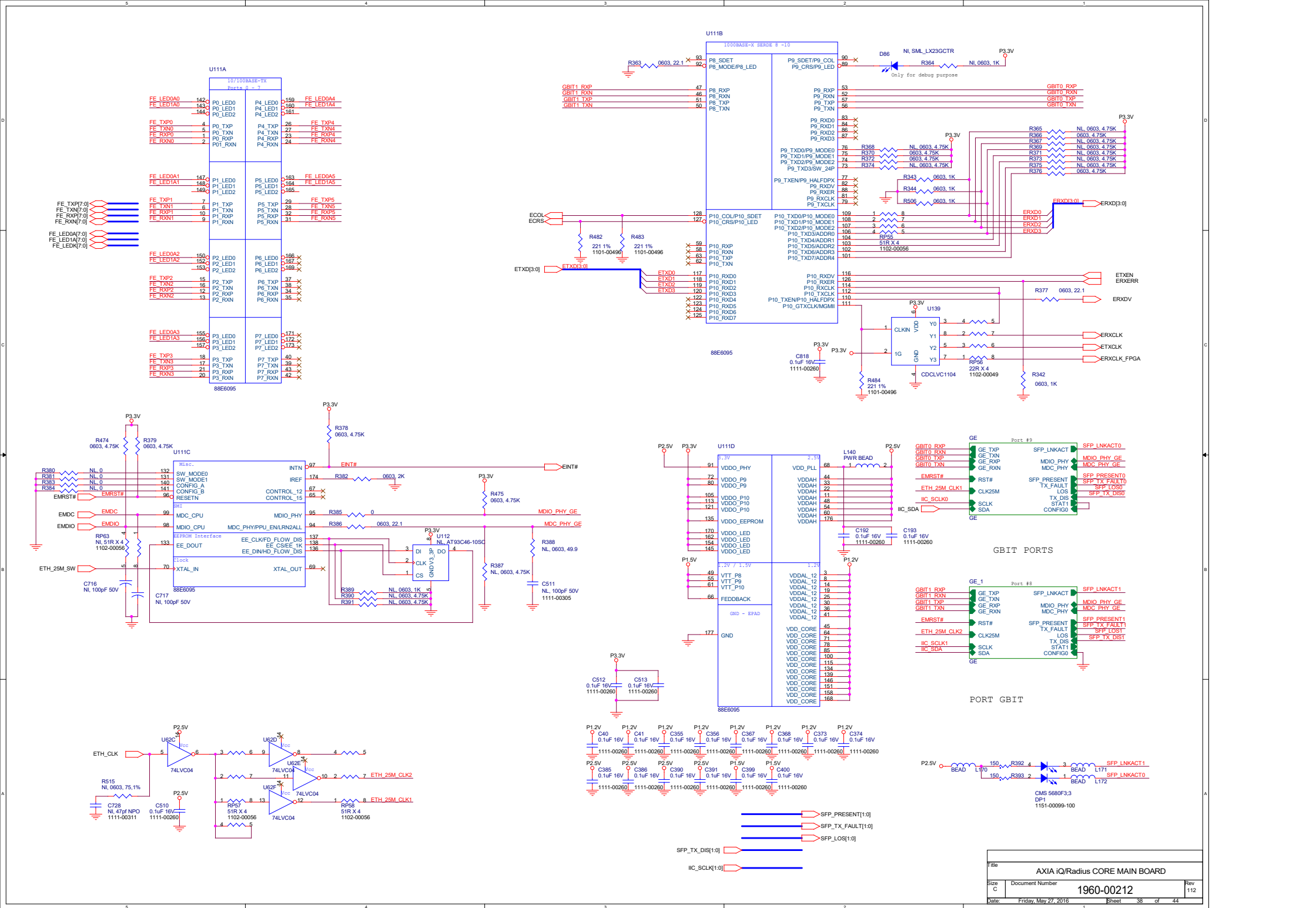
Gain = -15.85 dB (0.1613)



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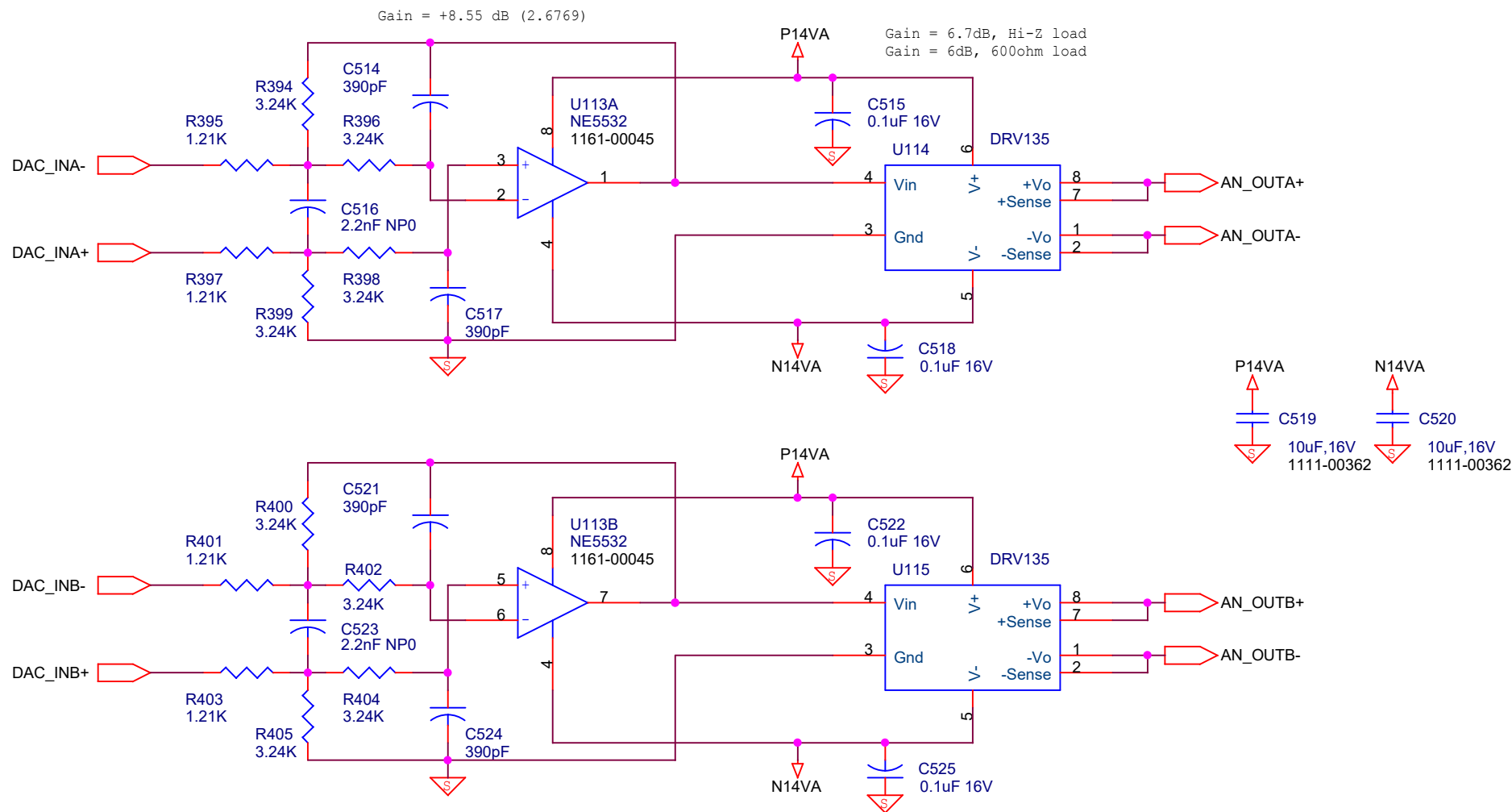




0 dBFS = 6.5 VPP = 2.3 VRMS

0 dBFS = 17.40 VPP = 6.15 VRMS

0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS



Title

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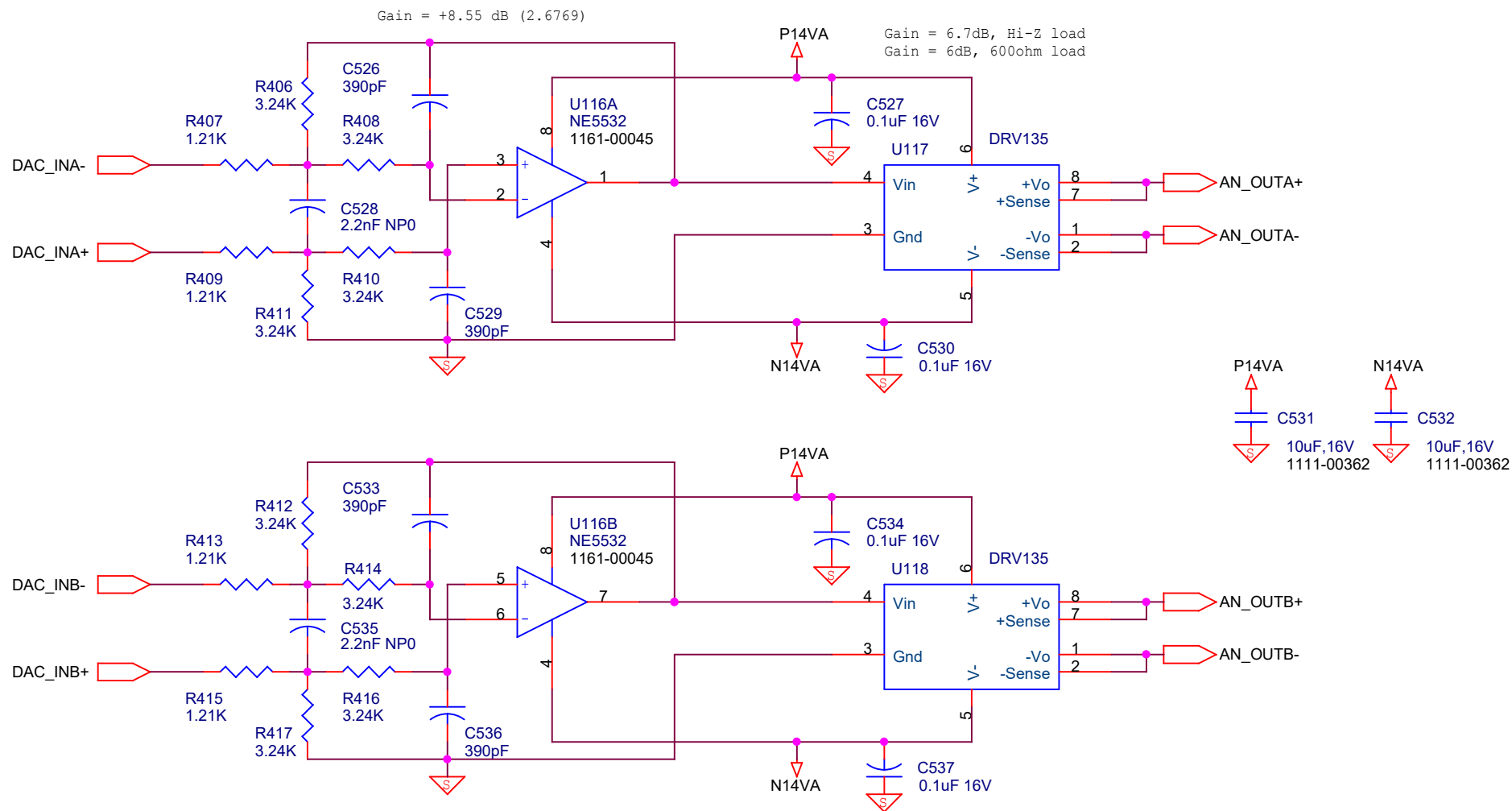
Date: Friday, May 27, 2016

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0 dBFS = 6.5 VPP = 2.3 VRMS

0 dBFS = 17.40 VPP = 6.15 VRMS

0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

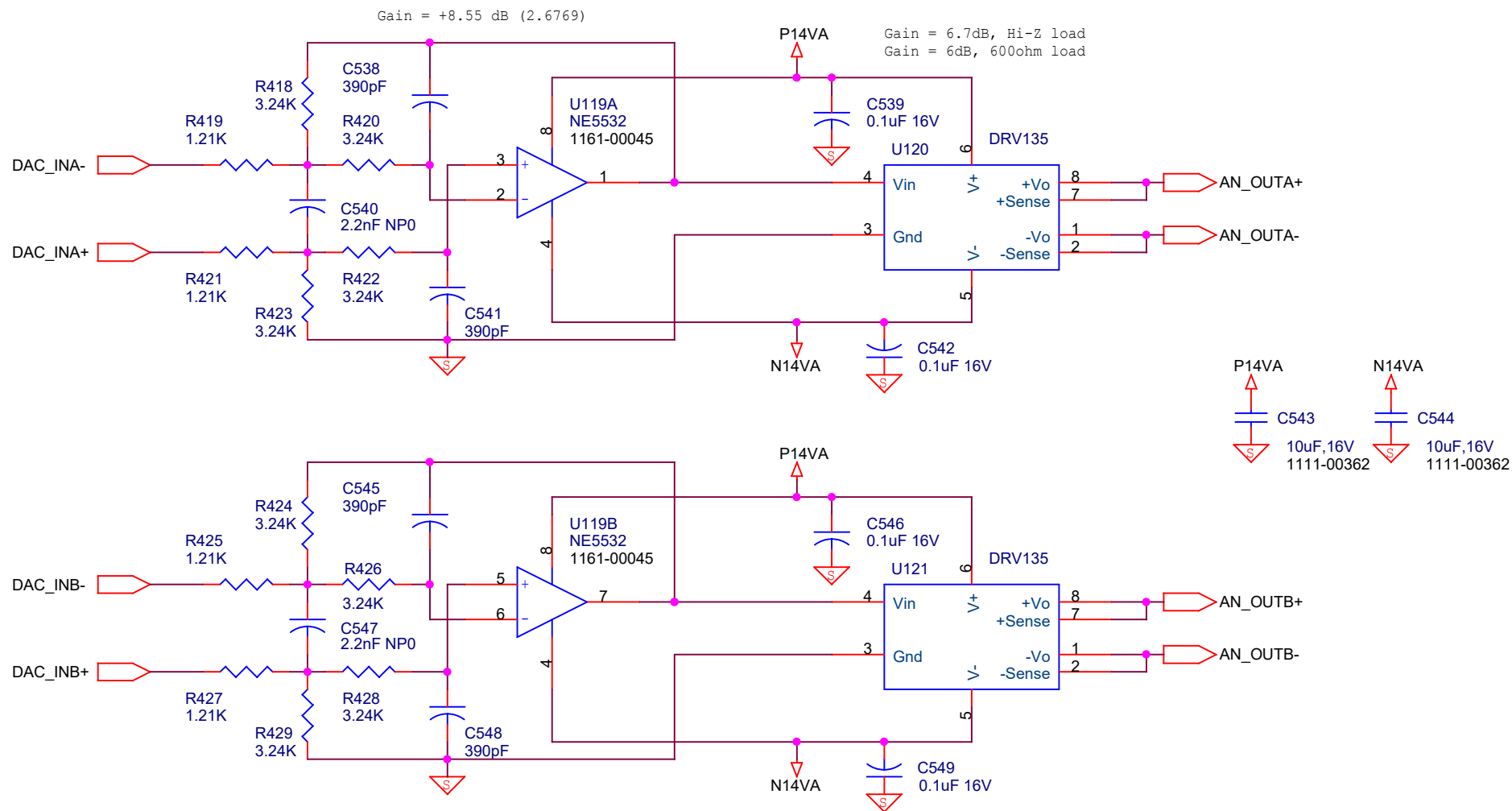


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AXIA iQ/Radius CORE MAIN BOARD		
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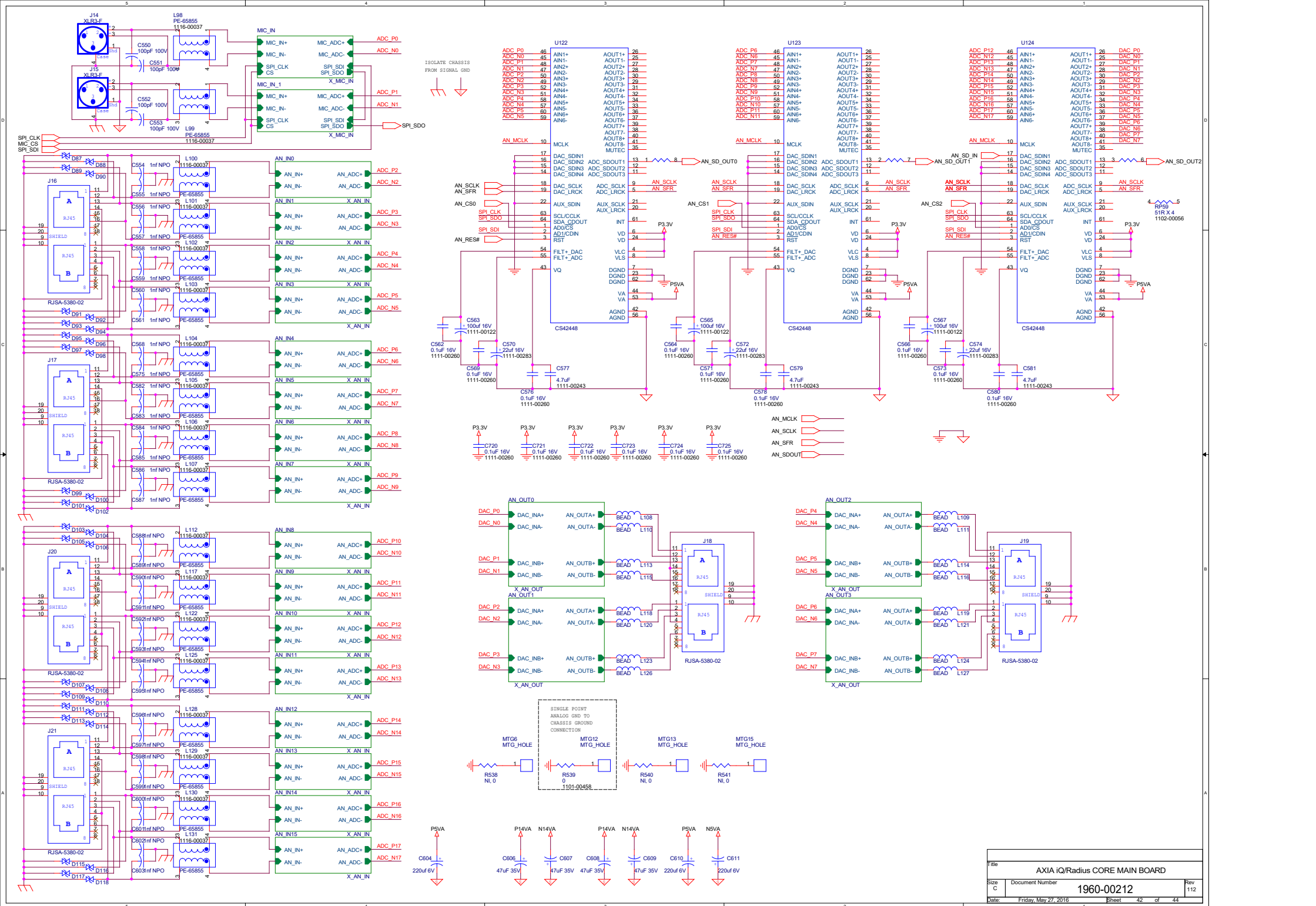
0 dBFS = 6.5 VPP = 2.3 VRMS

0 dBFS = 17.40 VPP = 6.15 VRMS

0 dBFS = +24.0 dBu = 34.72 VPP = 12.28 VRMS

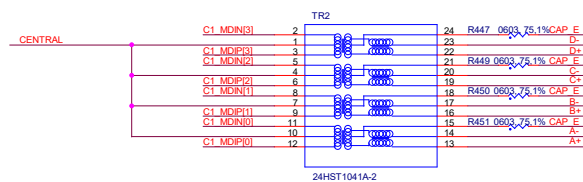
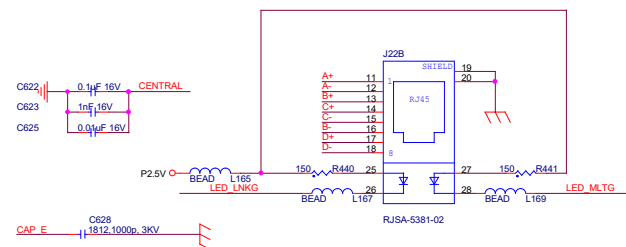
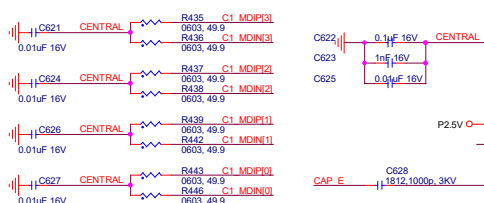


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AXIA iQ/Radius CORE MAIN BOARD		
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CONFIG1	VSS	2'b00
CONFIG2	VSS	2'b00
CONFIG3	VSS	2'b00
CONFIG4	VSS	2'b00
CONFIG5	VDDO C1	2'b11

```
*PHY ID = 0x00/0x01
(depend of "CONFIG0"
input)
```



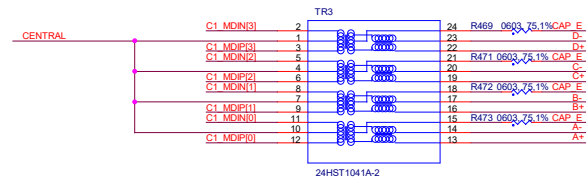
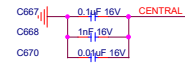
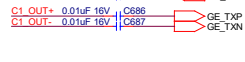
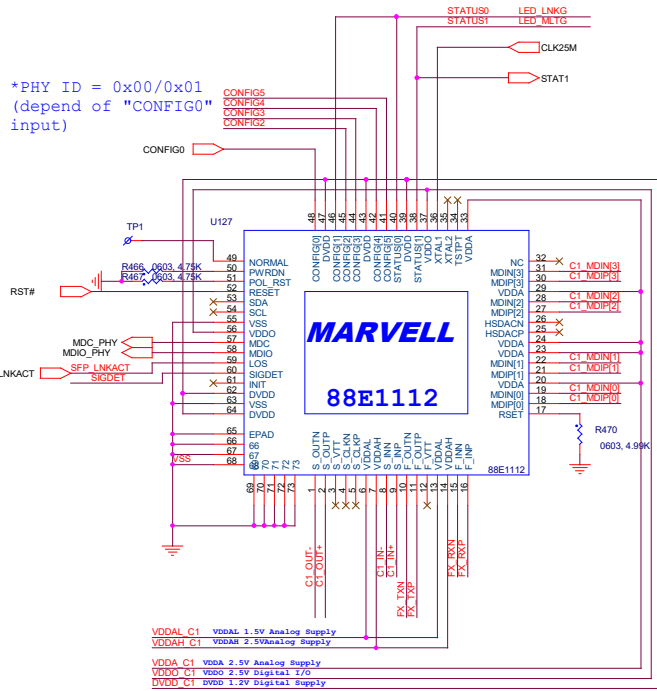
The diagrams illustrate the following decoupling capacitor placement schemes:

- P1.2V:** A capacitor labeled **DDVD C1** is connected to ground. Other components shown include C633, C634, C635, and C636, with values of 1uF 16V and 0.1uF 16V.
- P1.5V L134:** A capacitor labeled **VDDAL C1** is connected to ground. Other components shown include C643, C644, C645, and C646, with values of 1uF 16V and 0.1uF 16V.
- P2.5V L135:** A capacitor labeled **VDDAH C1** is connected to ground. Other components shown include C647, C648, C649, C650, and C651, with values of 1uF 16V and 0.1uF 16V.
- P2.5V:** A capacitor labeled **VDDO C1** is connected to ground. Other components shown include C654, C655, and C656, with values of 1uF 16V and 0.1uF 16V.

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CONFIG[0]	PHYADR[1]	PHYADR[0]
CONFIG[1]	PHYADR[3]	PHYADR[2]
CONFIG[2]	SGMII_CLK	PHYADR[4]
CONFIG[3]	SEL_TWSI	SEL_VTT
CONFIG[4]	EEPROM[1]	EEPROM[0]
CONFIG[5]	MODE[1]	MODE[0]

CONFIG1	VSS	2'b00
CONFIG2	VSS	2'b00
CONFIG3	VSS	2'b00
CONFIG4	VSS	2'b00
CONFIG5	VDDO C1	2'b11



The diagrams illustrate the placement of decoupling capacitors for three different power pins:

- P1.2V:** Shows a capacitor C678 (1uF 16V) connected to the PWR BEAD and a capacitor C679 (0.1uF 16V) connected to the VDDO C1 pin. A capacitor C680 (0.1uF 16V) is also shown connected to the VDDO C1 pin.
- P1.5V L138:** Shows a capacitor C688 (1uF 16V) connected to the PWR BEAD and a capacitor C689 (0.1uF 16V) connected to the VDDO C1 pin. A capacitor C690 (0.1uF 16V) is also shown connected to the VDDO C1 pin.
- P2.5V L139:** Shows a capacitor C691 (1uF 16V) connected to the PWR BEAD and a capacitor C692 (0.1uF 16V) connected to the VDDO C1 pin. A capacitor C693 (0.1uF 16V) is also shown connected to the VDDO C1 pin. A capacitor C694 (0.1uF 16V) is shown connected to the CENTRAL pin. A capacitor C695 (0.1uF 16V) is shown connected to the CENTRAL pin.

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